Closed-Loop Split-Phase Control Applied to a Regulating Point-of-Load (PoL) Dickson-Type Converter



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Motivation and Application

Hybrid Switched Capacitor (HSC) power converter topologies are being adopted in 48V to point-of-load (PoL) applications. Within the HSC converter class, Dickson-type converters [1] achieve the lowest Volt-Amp switch stress, indicative of a smaller semiconductor footprint for equivalent performance. However, some of these topologies require a non-conventional clocking scheme — recently coined as "split-phase switching" [2] — to ensure high efficiency is preserved. Executed in parallel with complimentary work in [3], this work presents a closed-loop split-phase control appropriate for regulating PoL converters [4]; over-coming a key obstacle to the deployment of a new and highly competitive class of hybridized power converter topologies.

Closed-loop Split-phase Control Demonstrated in Hardware



An added <u>Split-Phase Control Loop</u> detects "hard-charging" events and informs appropriate phase timing adjustments within a conventional FPGA-based clock generator.

[1] N. Ellis, R. Amirtharajah, "Large Signal Analysis on Variations of the Hybridized Dickson Switched-Capacitor Converter," TPEL 2022.
[2] Y. Lei, et. al., "Split-Phase Control: Achieving Complete Soft-Charging Operation of a Dickson Switched-Capacitor Converter," TPEL 2015.

[3] R. Abramson, et. al., "An Active Split-Phase Control Technique for Hybrid Switched-Capacitor Converters Using Capacitor Voltage Discontinuity Detection," COMPEL 2023.
[4] N. Ellis, et. al., "Closed-Loop Split-Phase Control Applied to the Symmetric Dual Inductor Hybrid (SDIH) Converter," COMPEL 2023.

Example: Phase Progression of the SDIH (Dickson-Type) Converter^[4]



The duration of all phases are fully constrained as a function of V_{IN} , V_{OUT} , I_{IN} , f_{SW} , & component values. The practical inclusion of loss and component derating/mismatch necessitates continuous and dynamic phase duration adjustments.



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