BPEC Mission

Berkeley Power and Energy Center

The mission of the Berkeley Power and Energy Center is to further research and education in the power and energy area through engagement with industry. We seek to create an eco-system where leading academic researchers and top industry partners can share and exchange ideas in pre-competitive areas, advance the frontier of technology, and help educate the next generation of technology leaders in industry and academia.

BPEC Faculty

Berkeley Power and Energy Center

Prof. Robert Pilawa-Podgurski, Director and Acting Executive Director

Prof. Jessica Boles, Co-Director, Power Electronics

Prof. Duncan Callaway, Principal Investigator, Power Systems

Prof. Emeritus Seth Sanders, Principal Investigator, Power Electronics

Dr. Sascha von Meier, Principal Investigator, Power Systems

Prof. Costas Spanos, Principal Investigator, Energy Efficiency

BPEC Students

Berkeley Power and Energy Center

Dr. Nathan Ellis

Dr. Samantha Coday

Margaret Blackwell

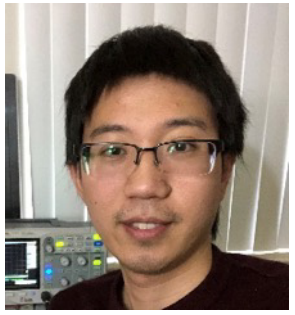
Rose Abramson

Nathan Brooks

Kelly Fernandez

Marrin Nerenberg

Logan Horowitz


Dr. Ting Ge

Rod Bayliss III

Yicheng Zhu

Rahul Iyer

Joseph Schaadt

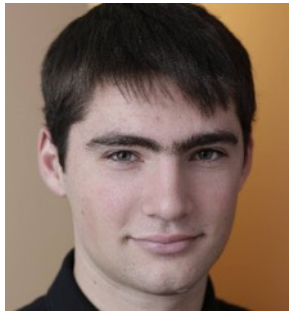
Sahana Krishnan

Jiarui Zou

Haifah Sambo

Francesca Giardine

Ben Liao


Nathan Biesterfeld

Elisa Krause

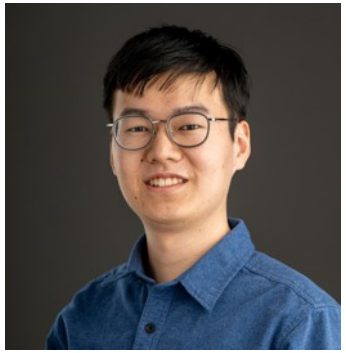
Nagesh Patle

BPEC Students

Berkeley Power and Energy Center

Tucker Skinner

Sourav Naval



Wentao Xu

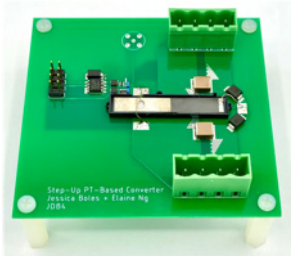
Dr. Mustapha Touhami

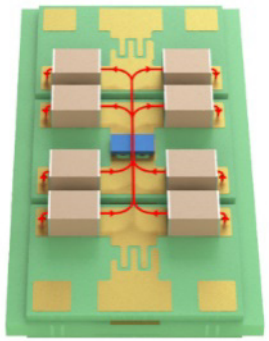
Tahmid Mahbub

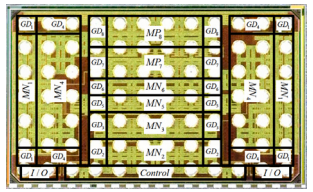
Research Programs

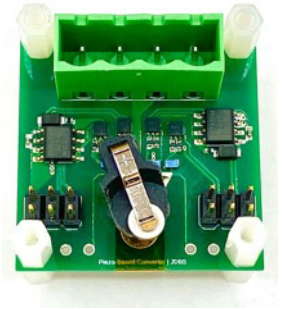
Berkeley Power and Energy Center

- Power Components and Devices

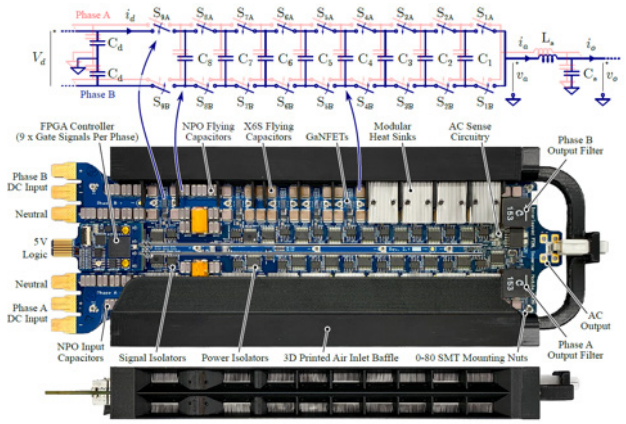


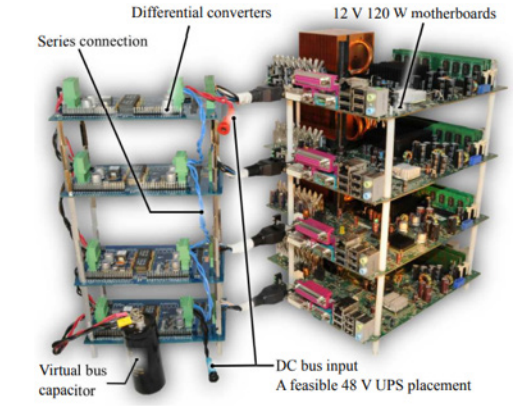




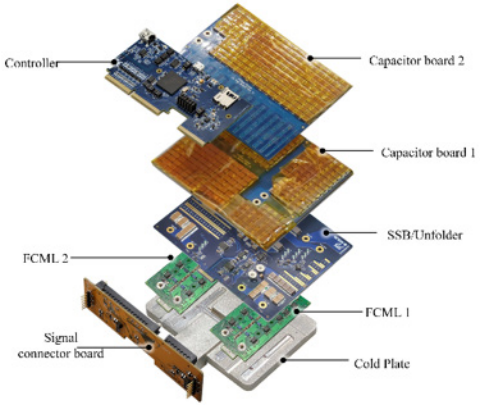


- Circuit Topologies and Control



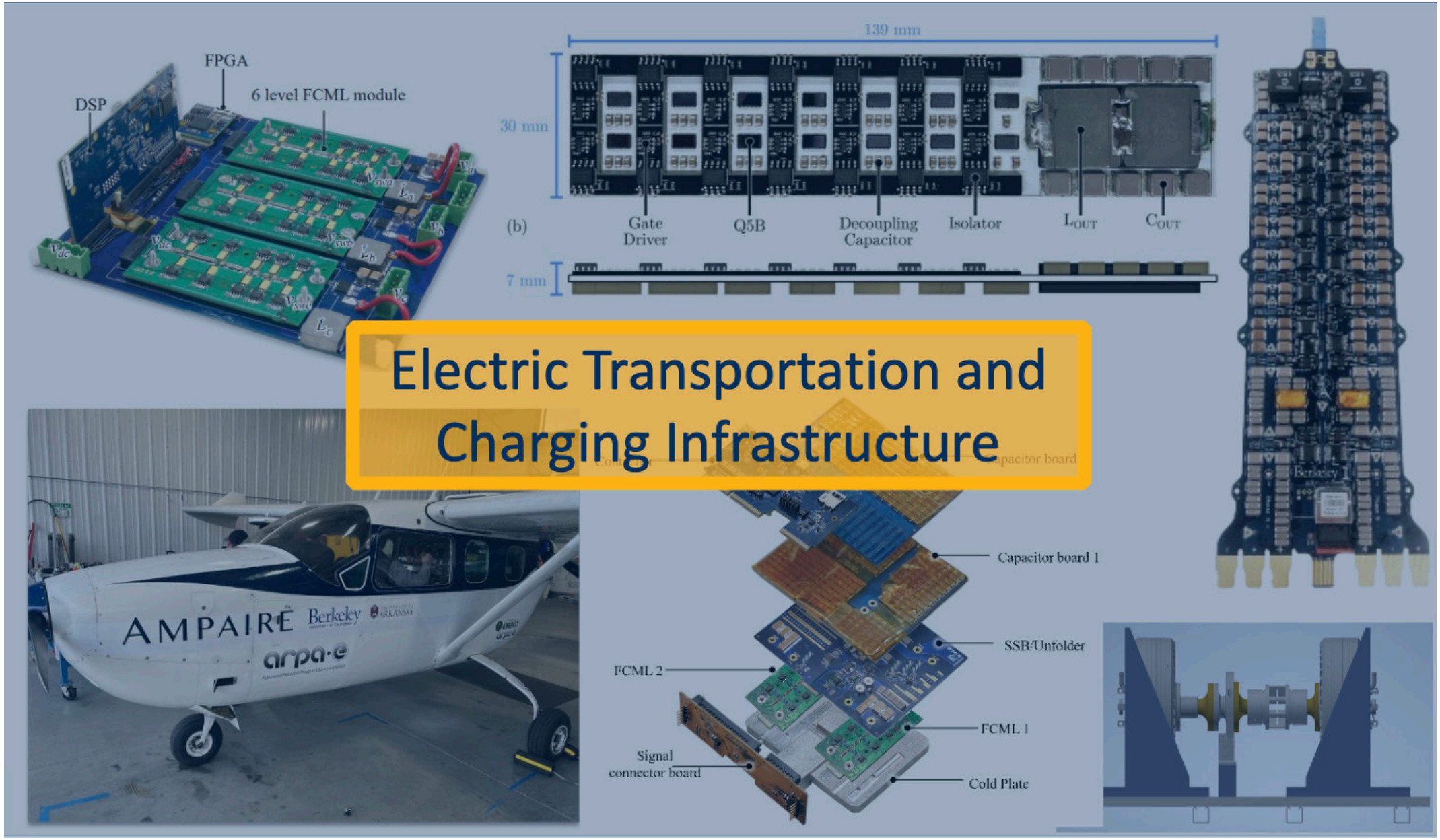


- Grid Integration – Systems and Technologies

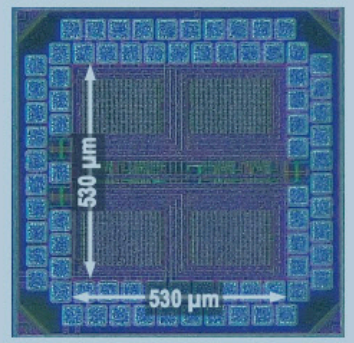


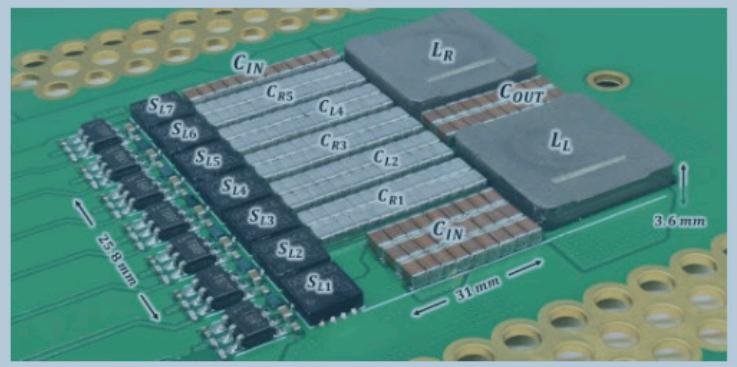
Application Areas

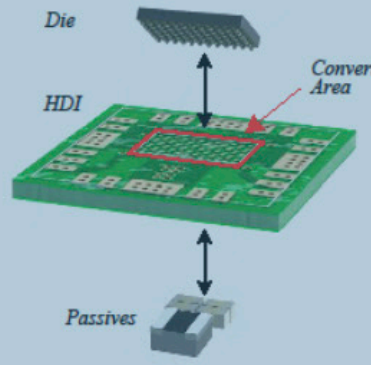
Berkeley Power and Energy Center



Application Areas







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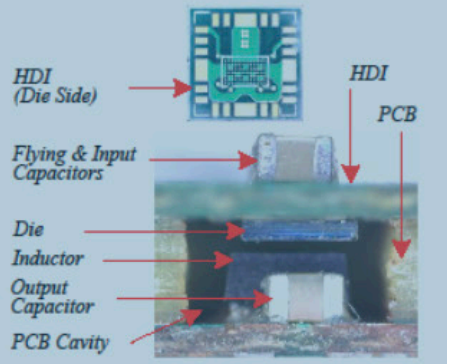

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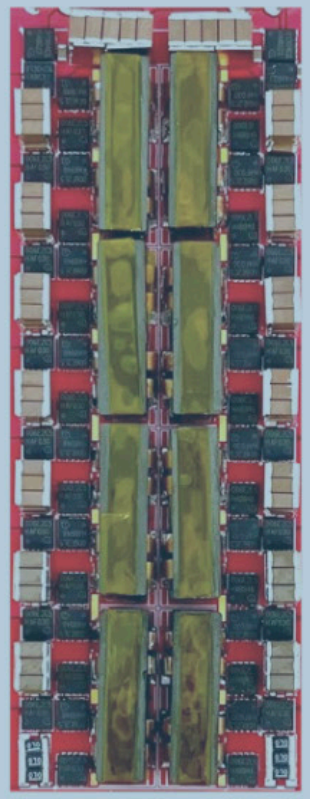
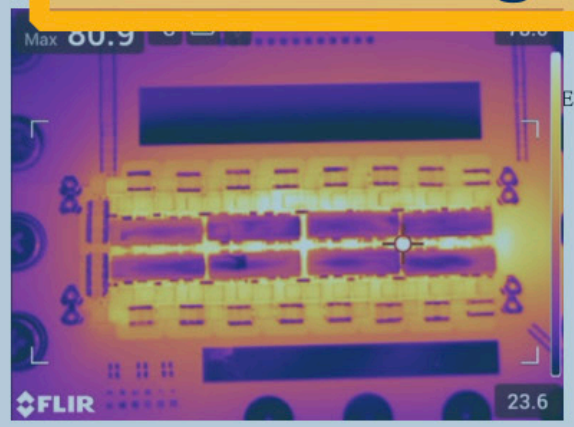
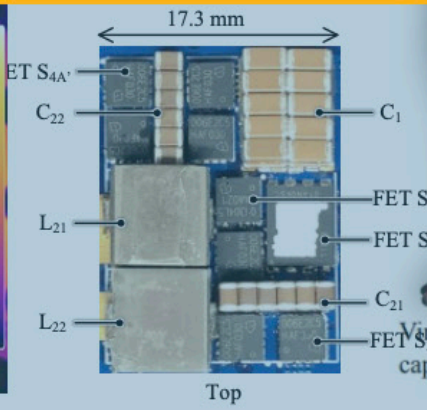
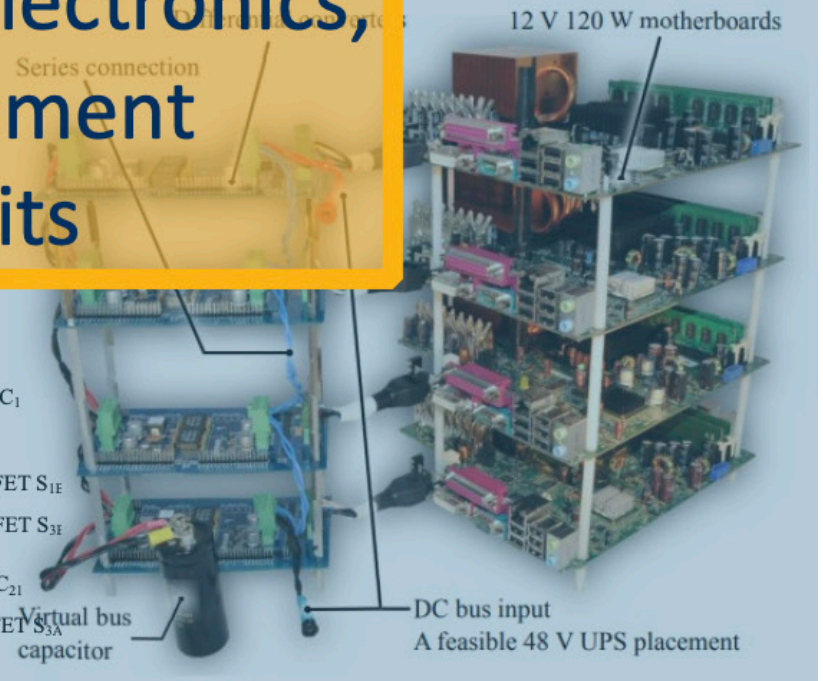


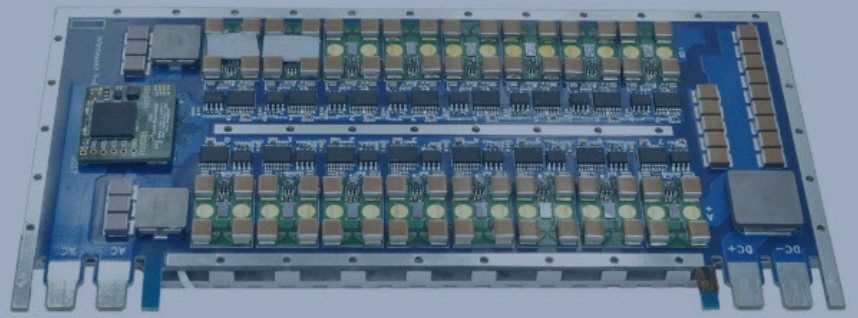
Datacenter, Consumer Electronics, and Power Management Integrated Circuits

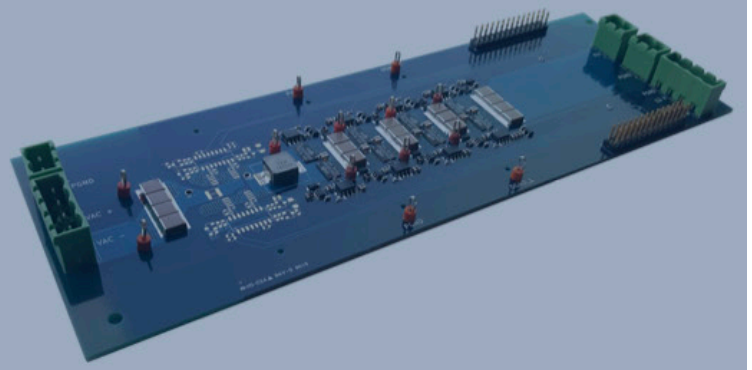




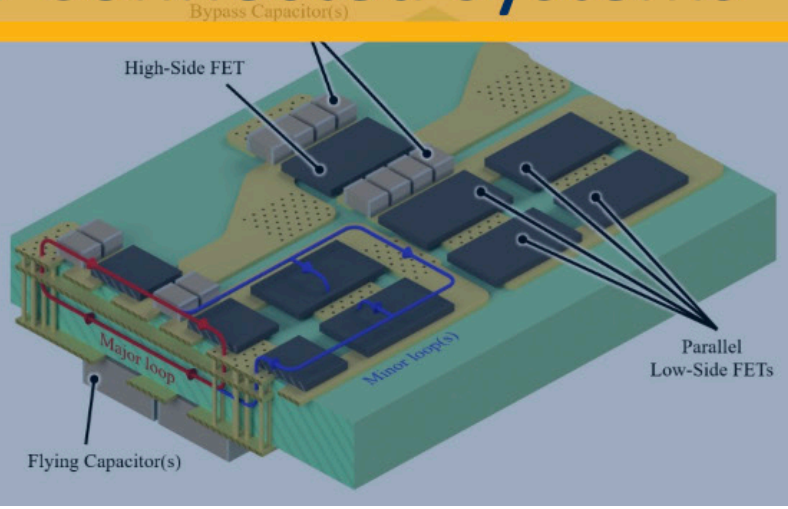


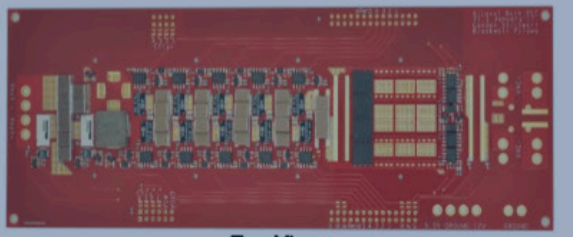
Application Areas





Renewables, Storage, and Grid-Connected Systems

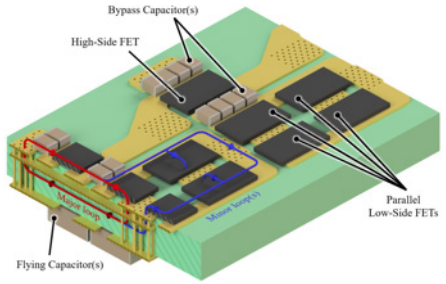


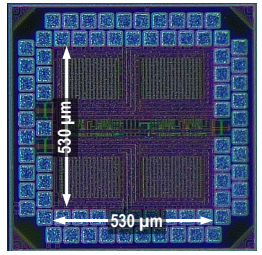


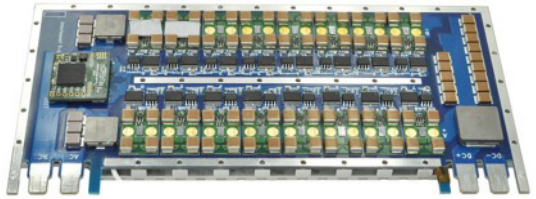
Membership Benefits

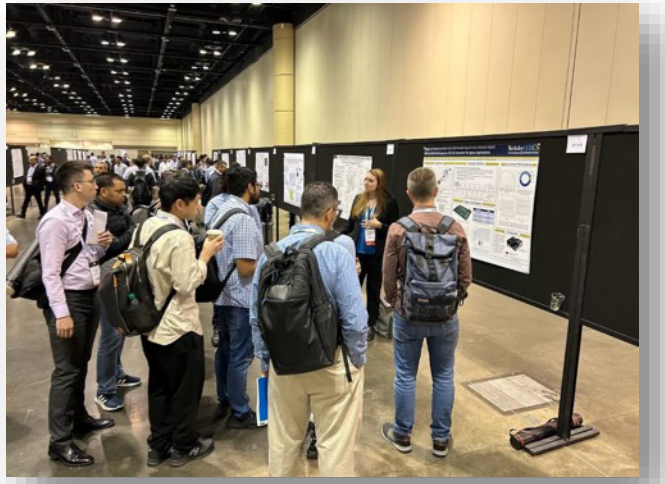
Berkeley Power and Energy Center

- Intellectual property rights to all inventions from BPEC sponsored research
- Early access to inventions and pre-publications
- Attendance at annual research review meetings at UC Berkeley campus
- Representation on Industrial Advisory Board
- Access to electronically archived BPEC theses, papers, presentations, tutorials, and webinars





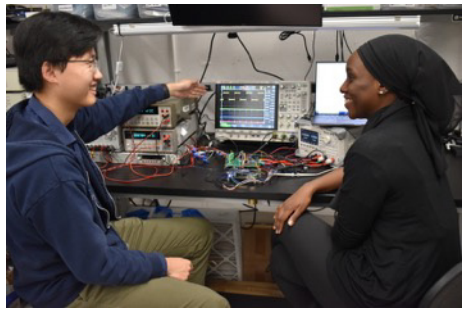


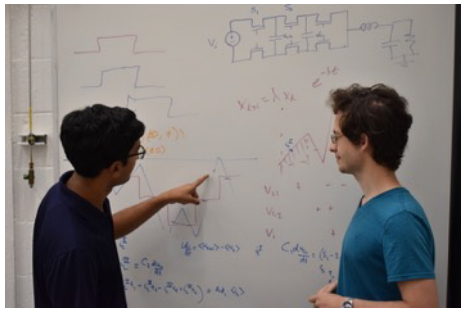


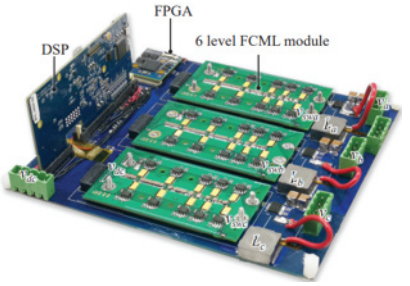
Membership Benefits

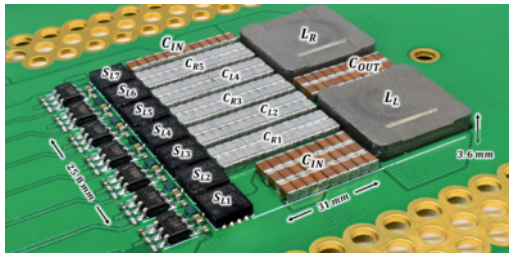
Berkeley Power and Energy Center

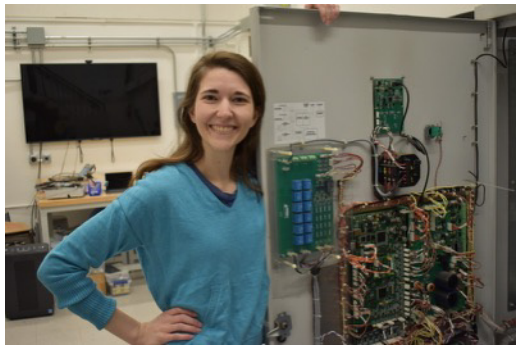
- Opportunity to direct funding to projects of particular interest to sponsor
- Opportunity to send Visiting Industrial Fellow to BPEC
- Access to students and faculty for research discussions and visits
- Resume book for all BPEC graduate and undergraduate students
- Opportunity to advertise career opportunities to power and energy courses
- Educational tutorials on topics of interest to industry







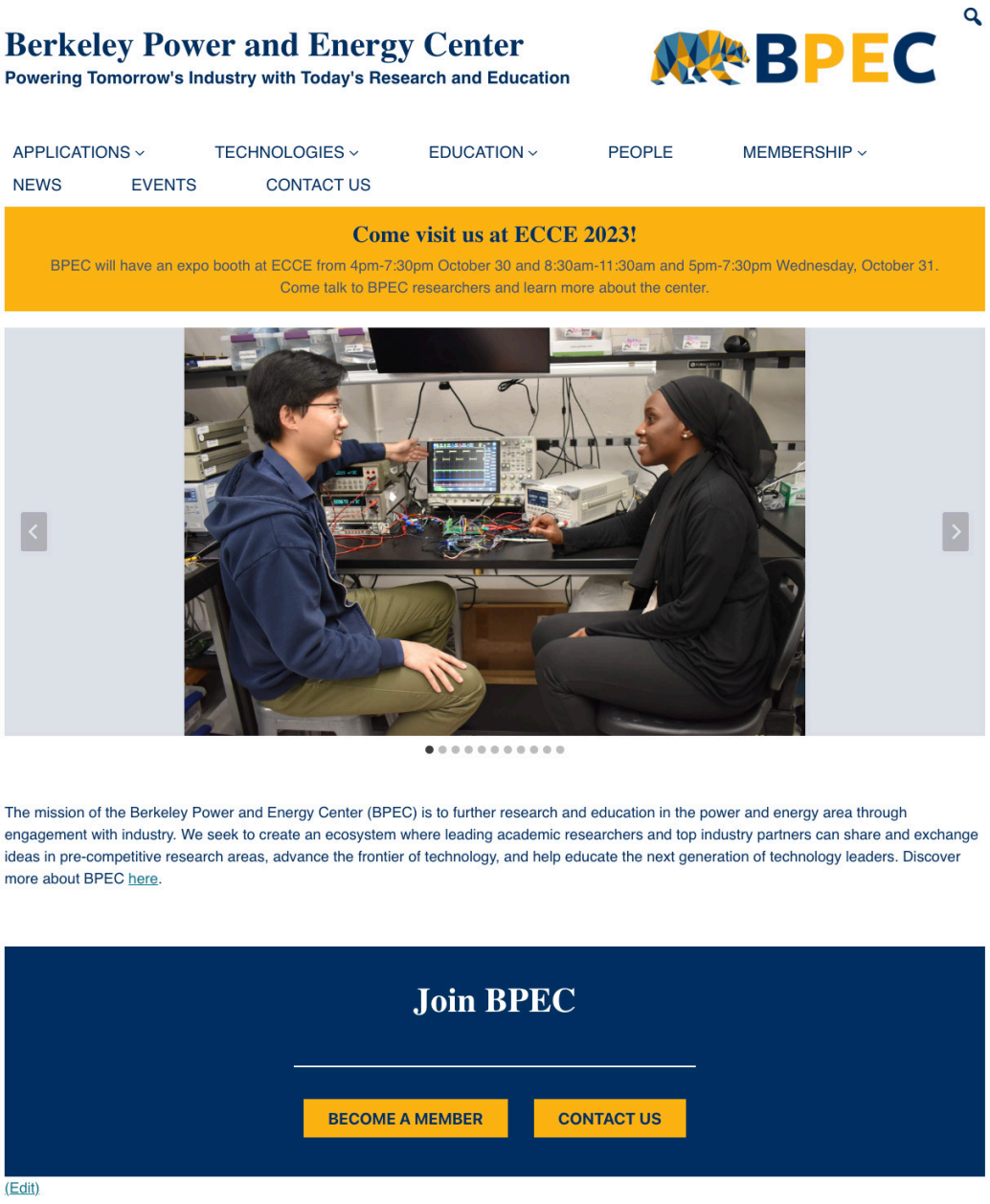




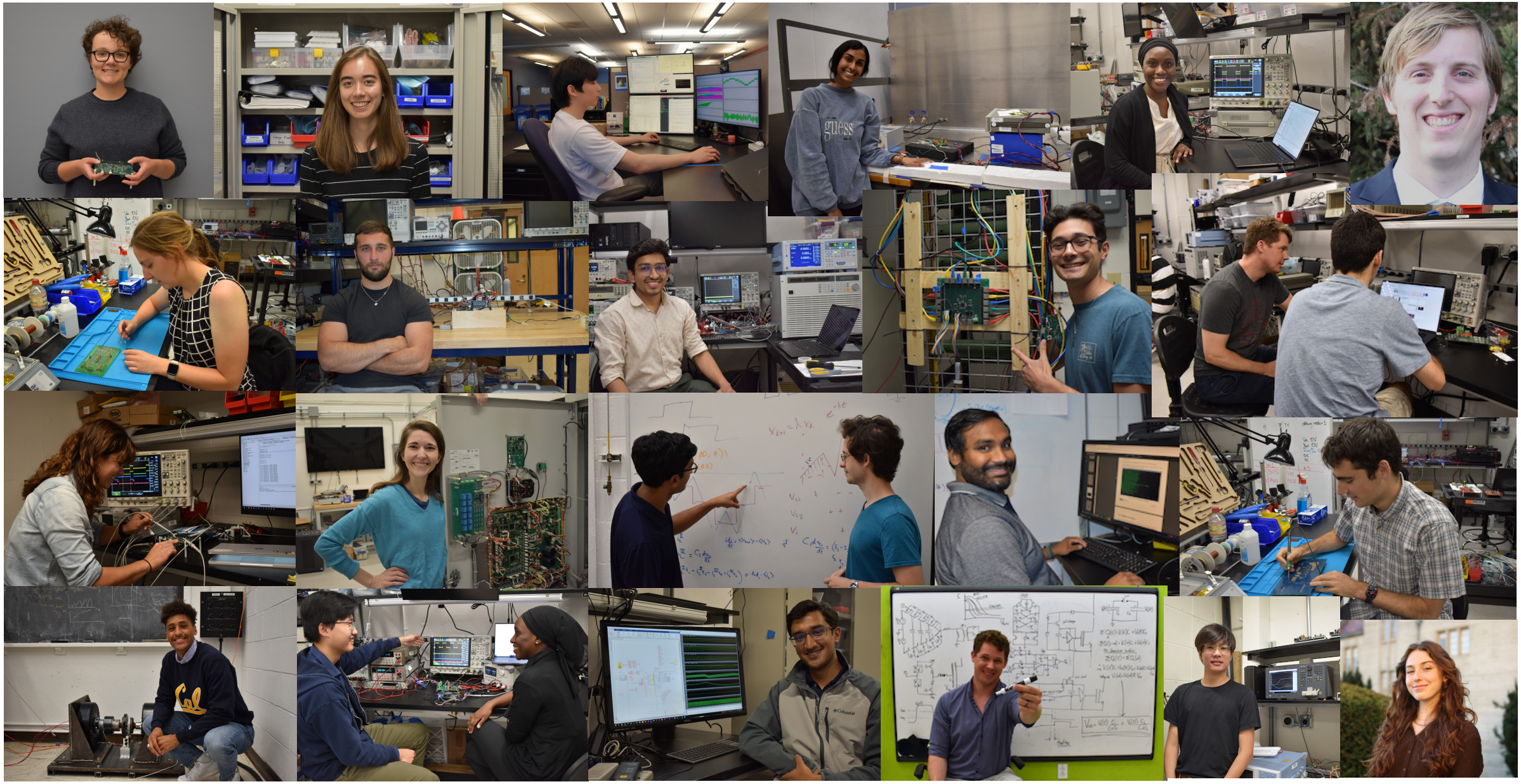
Membership levels

Berkeley Power and Energy Center

- Regular Member: $60,000 annually
- Collaborative Member (CM): $160,000 annually
  - Ability to directly support a Collaboration Membership Supported Project, in an area of interest to sponsor
- Additional CM projects: $100,000 annually
- For more information and how to join, please visit bpec.berkeley.edu



BPEC - Powering Tomorrow's Industry with Today's Research and Education

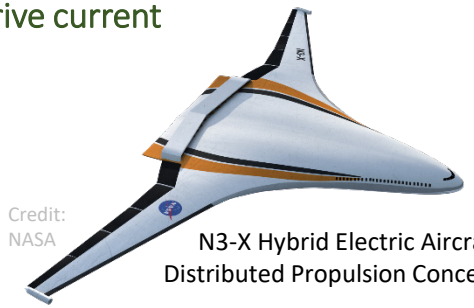


Extreme Performance Scalable Inverter Architecture for More Electric Aircraft (MEA) Propulsion

Berkeley Power and Energy Center

Motivation and Application

- Commercial aviation benefits from electric & hybrid vehicles
- Electric engines can be quieter and cleaner than jet engines
- Electric drive system must be power-dense and efficient
- Advanced power dense motors[2] need low THD, high frequency drive current



Credit: NASA

N3-X Hybrid Electric Aircraft Distributed Propulsion Concept

University of Illinois 1 MW Motor Concept [2]

NASA MEA Roadmap [1]

NOx emissions

80%

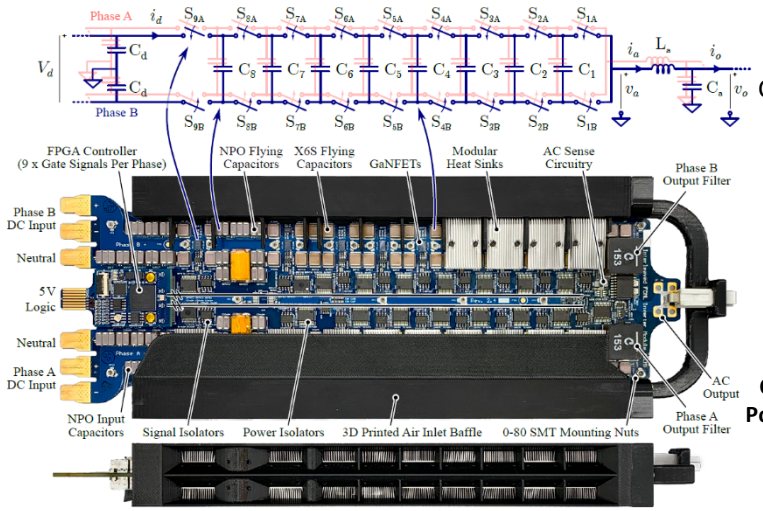
fuel consumption

60%

acoustic noise

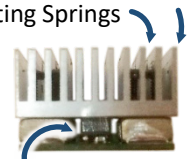
71dB

Electrical, Mechanical and Thermal Management Hardware

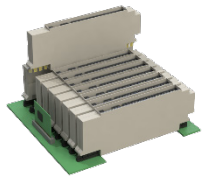


Load Shedding

CFD-Optimized Heat Sink Mounting Springs



GaN Device



Thermal Design Impacts

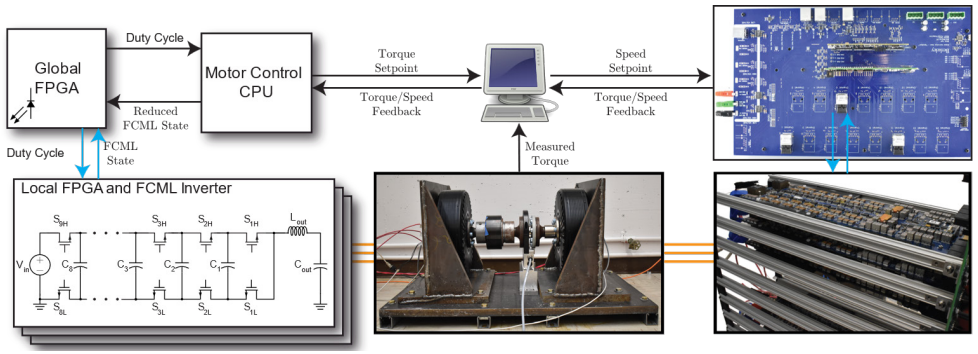
Chip-Scale GaN Power Transistors → Compact Layout → Faster Switching

New Cooling Challenges

Higher Power Density

High Power Dynamometer

- Dyno incorporates two low-inductance Emrax 348 machines (peak power: 260 kW)
- Testing validated the Flying Capacitor Multilevel Converter's (FCML) strength in a realistic motor drive system



Experimental Verification or Other

- Prototype meets NASA performance metrics for turbo-electric aircraft [4]
- Integration of advanced thermal management will boost maximum output power and efficiency
- Modular design provides for power scalability and fault resiliency
- Next steps: verification of floating-point motor control algorithm and high-power dyno and next generation inverter hardware development

	NASA Target	This Work
Peak Efficiency	99%	98.95%
Power Density	19 kW/kg	38.4 kW/kg

References:
N. Pallo, R. S. Bayliss and R. C. N. Pilawa-Podgurski, "A Multi-Phase Segmented Drive Comprising Arrayed Flying Capacitor Multi-Level Modules," IEEE APEC 2021
[1] N. Madavan, et al., "A NASA Perspective on Electric Propulsion Technologies for Commercial Aviation," 2016.
[2] X. Zhang and K. Haran, "High-Specific-Power Electric Machines for Electrified Transportation Applications Technology Options," IEEE ECCE 2016.
[3] N. Pallo, et al., "Power-Dense Multilevel Inverter Module using Interleaved GaN-Based Phases for Electric Aircraft Propulsion," IEEE APEC 2018.
[4] N. Pallo, C. Kharangate, et al., "Modular Heat Sink for Chip-Scale GaN Transistors in Multilevel Converters," IEEE APEC 2018.

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Design of an Efficient, Lightweight Flying Capacitor Multilevel Converter for Electrified Flight

Berkeley Power and Energy Center

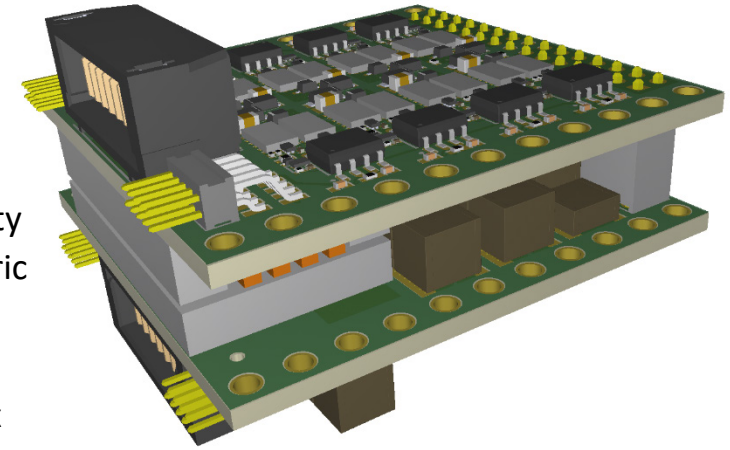
Motivation and Application

- Air travel accounts for ~200 million tons of CO_2 emissions annually (3% of US greenhouse gas emissions)[1]
- Air travel demand is expected to double every fifteen years
- Electrification of flight requires efficient, lightweight, and reliable power conversion
- Hardware must be flight qualified

Pictured: Ampaire Electric EEL flight

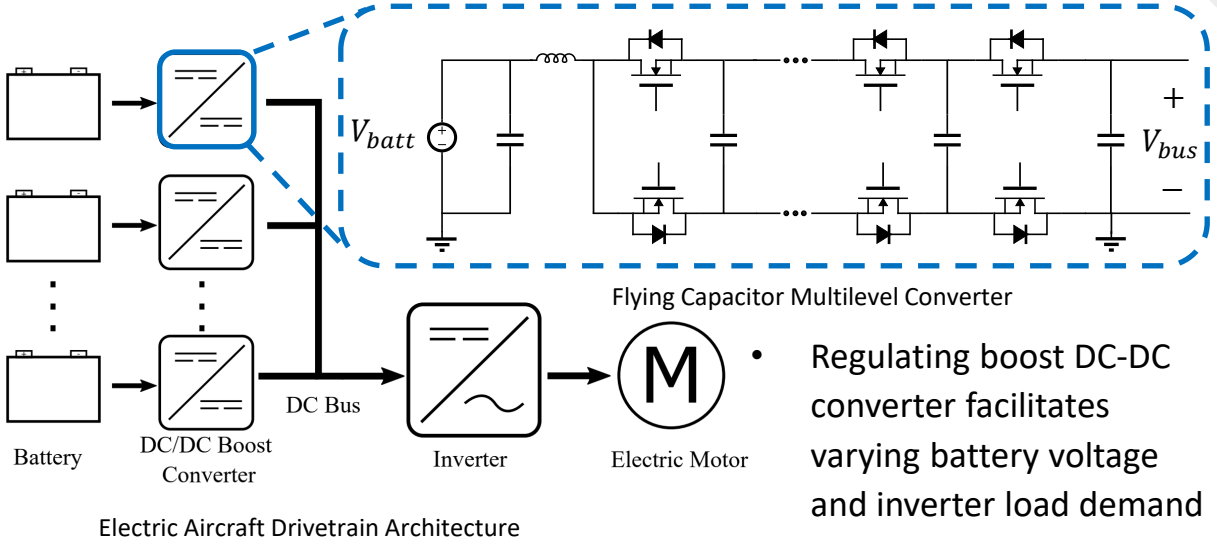
Hardware Prototype

- Snubbers enable decreased overlap loss without sacrificing conduction path
- Paralleled switches enable increased areal power density
- Derated energy density metric used to optimize flying capacitor part/count
- Custom inductor achieves 3x mass reduction



3D rendering of 8-level boost FCML prototype

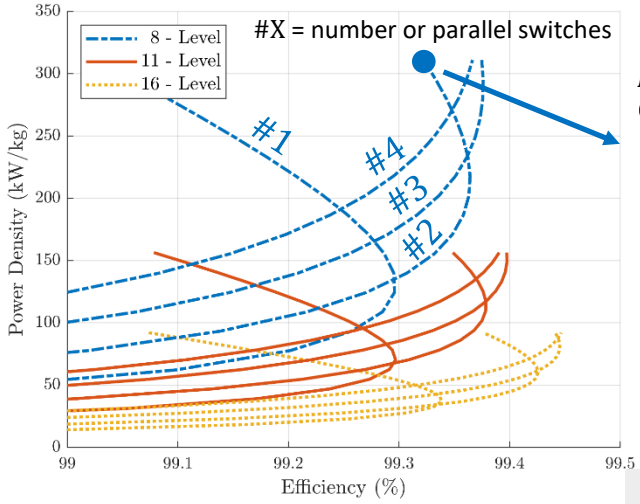
Proposed Solution

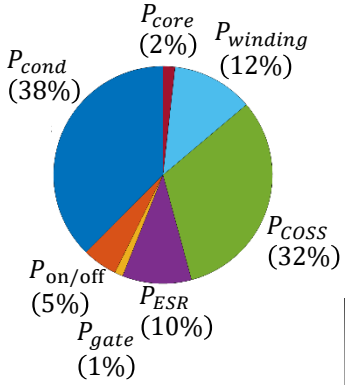


Electric Aircraft Drivetrain Architecture

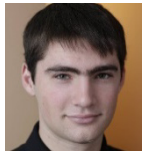
- Regulating boost DC-DC converter facilitates varying battery voltage and inverter load demand

Modeled Performance





Loss Breakdown



[1] https://www.epa.gov/greenvehicles/fast-facts-transportation-greenhouse-gas-emissions

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Rahul Iyer Email: rkiyer@berkeley.edu

Empowering Future Electric Aircraft with a Flying Capacitor Multilevel Inverter Utilizing Optimal Passive Components

Berkeley Power and Energy Center

Motivation and Application

- Air travel accounts for ~200 million tons of CO_2 emissions annually (3% of US greenhouse gas emissions)[1]
- Air travel demand doubles every fifteen years
- Electrification of flight requires efficient, lightweight, and reliable power conversion

Credit: Boeing

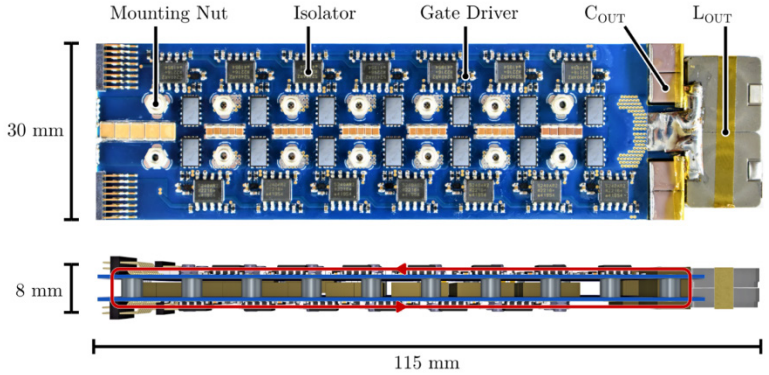
Credit: NASA

fuel consumption 60%

NOx emissions 80%

acoustic noise 71dB

Hardware Prototype

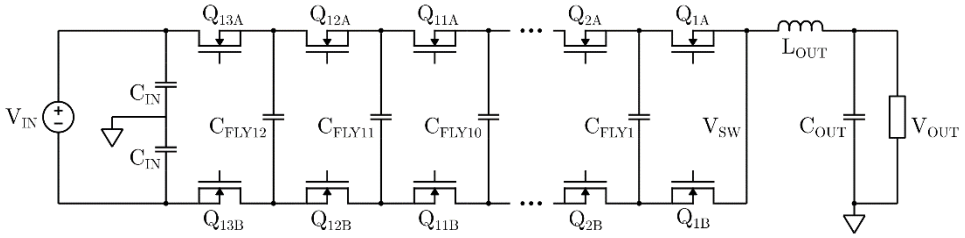


- 10 kW, 800 V, 14-level FCML
- Sandwich-style layout with two printed circuit boards
- Ultra-thin design, only 8 mm thick!

Key Converter Parameters	
Input Voltage	800 V_{DC}
Output Voltage	270 V_{RMS}
Effective Switching Frequency	1.95 MHz
Peak Output Power	10.3 kW
Peak Overall Efficiency	98.2 %
Gravimetric Density	170 kW/kg
Volumetric Density	370 kW/L

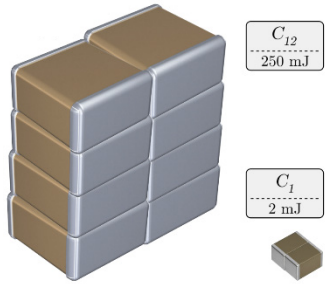
FCML with Optimal Passive Component Selection

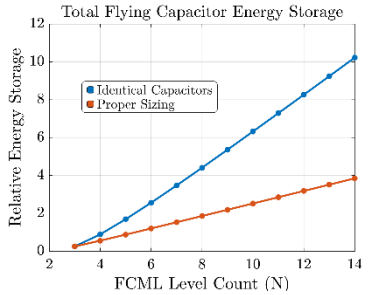
Simplified 14-level FCML schematic



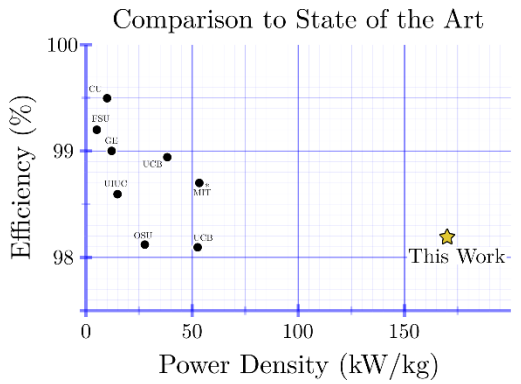
Capacitor Sizing

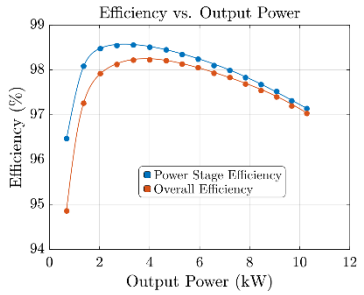
- Conventional approach utilizes large, identical capacitors
- Proposed approach optimally selects unique capacitors for each flying capacitance
- **Enables > 50% reduction in size**

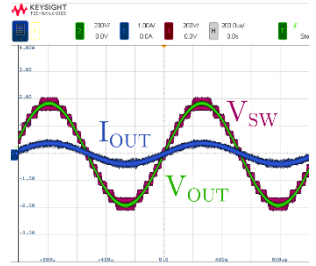




Experimental Verification







- **Highest power density** among state-of-the-art aircraft inverters
- Excellent capacitor balancing and **low output distortion** despite the small size of the converter

References:
[1] https://www.epa.gov/greenvehicles/fast-facts-transportation-greenhouse-gas-emissions

Logan Horowitz | Email: logan_h_horowitz@berkeley.edu

Tethered Power Systems for Lunar Mobility and Power Transmission (TYMPO)

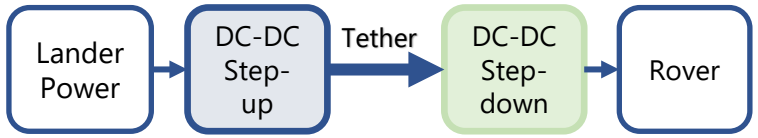
Berkeley Power and Energy Center

Motivation and Application

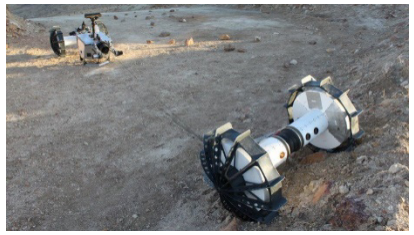
Extreme terrain capable robots will enable further exploration on sites such as pits on the moon and Martian landscape. Tethered power systems have been proposed to power these small rovers; however, they require high voltage DC power [1].

Challenges

High voltage switches are difficult to use in space due to radiation effects. Additionally, the high voltage conversion ratio makes it difficult to design a compact and efficient power converter. Therefore, multilevel topologies offer promising solutions [2].



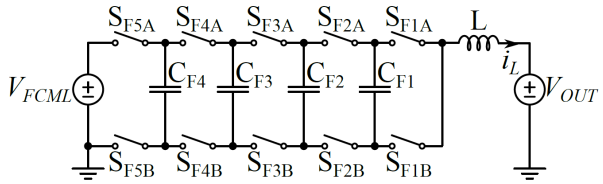
TYPMO architecture



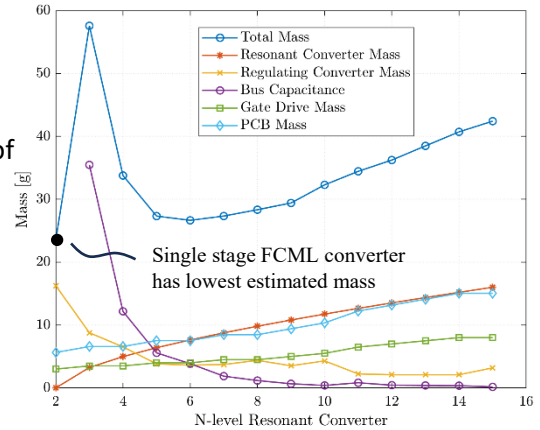
Tethered rover to explore lunar pits

System Architecture (Flying Capacitor Multilevel Converter)

- Comparison of cascaded structure consisting of resonant flying capacitor multilevel converter (FCML) and regulating FCML (resonant FCML + regulating FCML) vs single-stage FCML converter
- Bus capacitance requirement diminishes benefits of cascaded structure



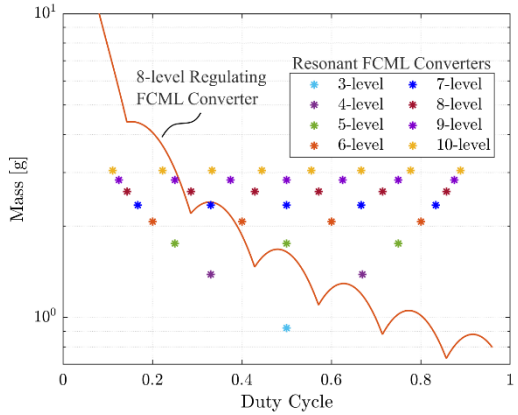
FCML converter schematic



Estimated mass breakdown of cascaded FCML converter structure

Passive Mass Minimization

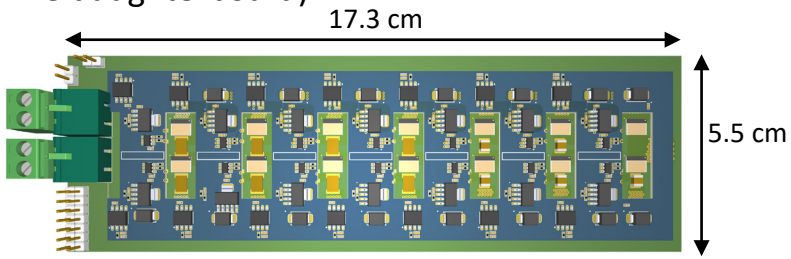
- Comparison of 8-level regulating mode FCML converter with a resonant mode FCML converter, demonstrating the advantages of a resonant converter in terms of passive component mass
- Each converter operating point is optimized for minimal mass based on the peak energy storage requirements of the passive components

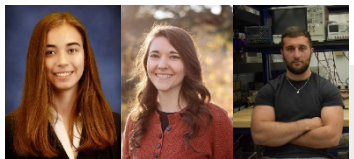


Hardware Verification

840 V-to-120 V space-rated FCML converter to verify:

- PCB structure (Gate drive daughterboard)
- Part selection
- Thermal solutions
- Mass optimization





Student: Elisa Krause, Maggie Blackwell, Logan Horowitz
Email: {elisa_Krause, blackwell, logan_h_horowitz}@berkeley.edu

References:
[1] P. McGarey, W. Reid and I. Nesnas, "Towards Articulated Mobility and Efficient Docking for the DuAxel Tethered Robot System," *2019 IEEE Aerospace Conference*, 2019, pp. 1-9.
[2] P. McGarey, T. Nguyen, T. Pailevanian and I. Nensas, "Design and Test of an Electromechanical Rover Tether for the Exploration of Vertical Lunar Pits," *2020 IEEE Aerospace Conference*, 2020, pp. 1-10.
[3] S. Coday, A. Barchowsky and R. C. N. Pilawa-Podgurski, "A 10-level GaN-based Flying Capacitor Multilevel Boost Converter for Radiation-Hardened Operation in Space Applications," *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 2798-2803.

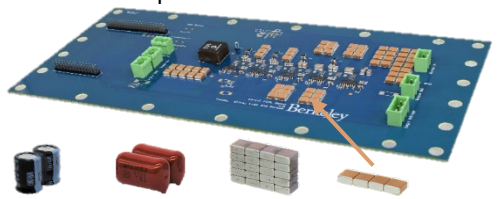
On the Size and Weight of Passive Components: Scaling Trends for High-Density Power Converter Designs

Berkeley Power and Energy Center

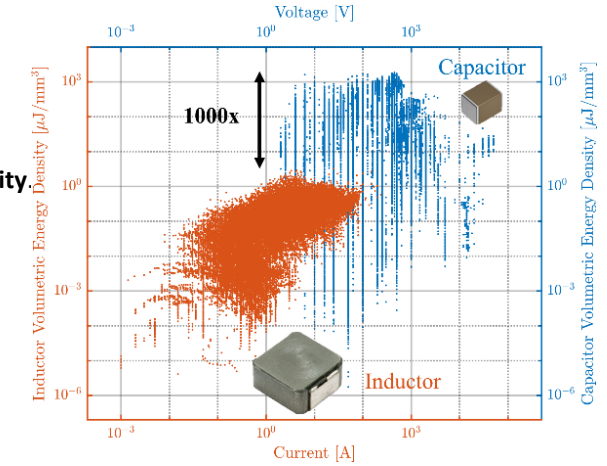
Motivation and Application

To build a high-density power converter, practicing engineers need to use passive components with the highest density.

- A component survey finds **Volumetric Energy Density**.
  - Visualized to assist component selection.
- But how to estimate **Gravimetric Energy Density**?
  - No component mass on most datasheet.

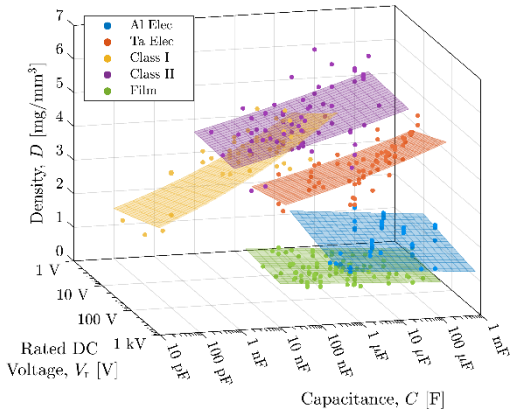


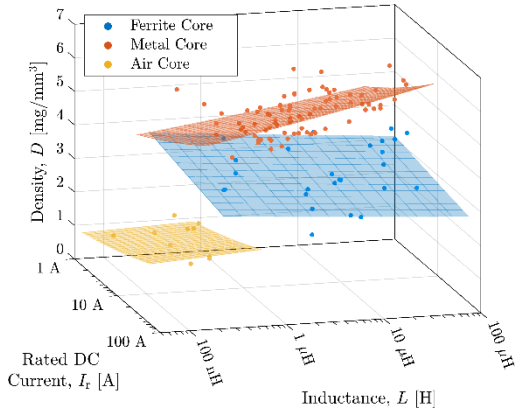
2 µF @ 450 V Aluminum Electrolytic | 2 µF @ 450V Polypropylene Metalized Film | 2 µF @ 450 V Class 1 Ceramic | 2 µF @ 450 V Class 2 Ceramic



Volumetric Energy Density determined by a component survey encompassing over **606,000 capacitors** and **88,000 inductors**

Power Fit Estimation for Specific Density (D)





$$D = k \cdot V_r^{\alpha} \cdot C^{\beta} \quad \left[\frac{mg}{mm^3}\right]$$

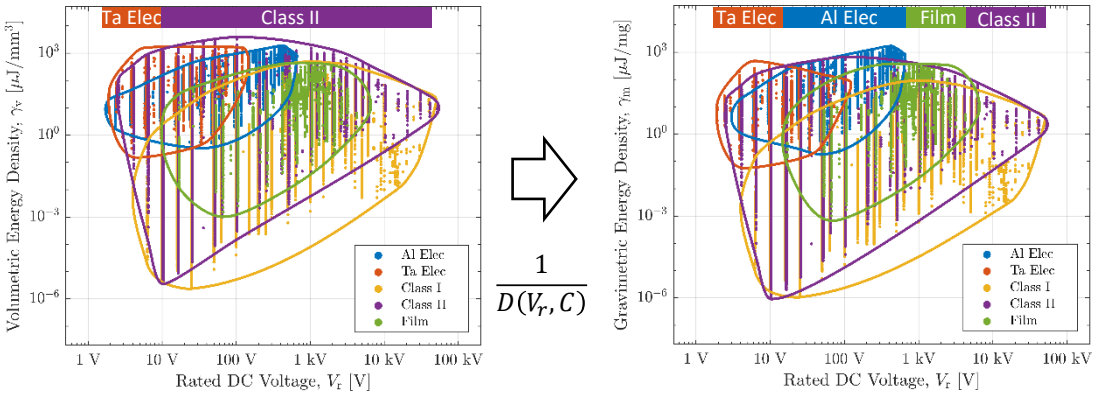
$$D = k \cdot I_r^{\alpha} \cdot L^{\beta} \quad \left[\frac{mg}{mm^3}\right]$$

Mass data was obtained through manual measurements of over **6,000 components**

Capacitor Volumetric vs. Gravimetric Energy Density

$$\rho_V = \frac{\frac{1}{2} C V_r^2}{Vol} = \left[\frac{J}{mm^3}\right] \qquad D(V_r, C) = \frac{Mass}{Vol} \qquad \rho_M = \frac{\frac{1}{2} C V_r^2}{Mass} = \left[\frac{J}{mg}\right]$$

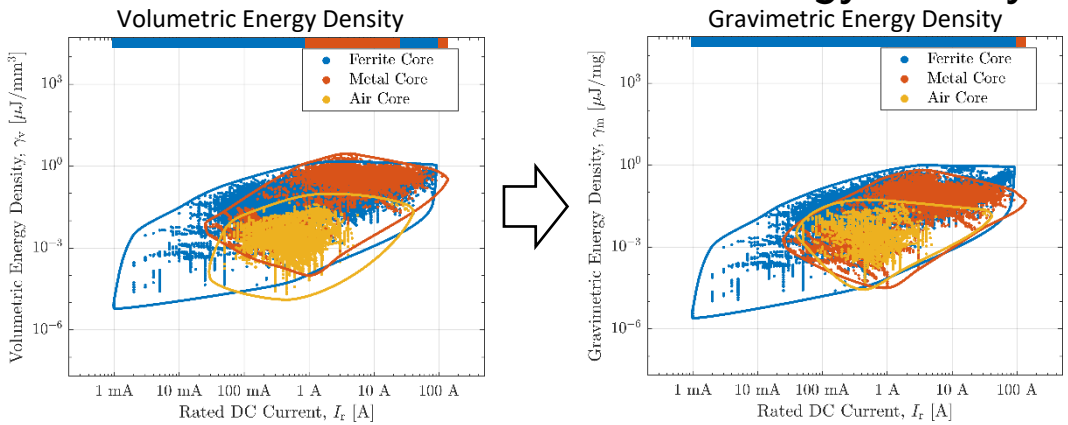
Volumetric Energy Density | Gravimetric Energy Density



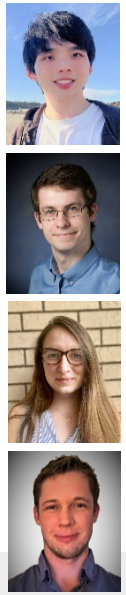
$$\frac{1}{D(V_r, C)}$$

Use **Specific Density (D)** to Derive **Gravimetric Energy Density** from **Volumetric Energy Density**

Inductor Volumetric vs. Gravimetric Energy Density



References: J. Zou, N. C. Brooks, S. Coday, N. M. Ellis and R. C. N. Pilawa-Podgurski, "On the Size and Weight of Passive Components: Scaling Trends for High-Density Power Converter Designs," 2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL), Tel Aviv, Israel, 2022, pp. 1-7, doi: 10.1109/COMPEL53829.2022.9829957.



Jiarui Zou, jiarui.zou@berkeley.edu; Nathan Brooks, nathanbrooks@berkeley.edu;
Samantha Coday, Scoday@berkeley.edu; Nathan Ellis, Nathanmilesellis@berkeley.edu

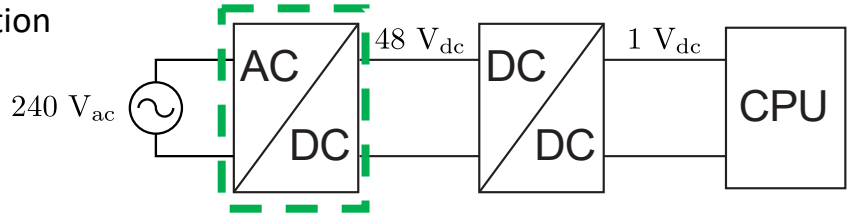
Enabling Buck-Type AC/DC Grid-Tied Rectifiers Using Flying Capacitor Multi-Level Converters with Advanced Control

Berkeley Power and Energy Center

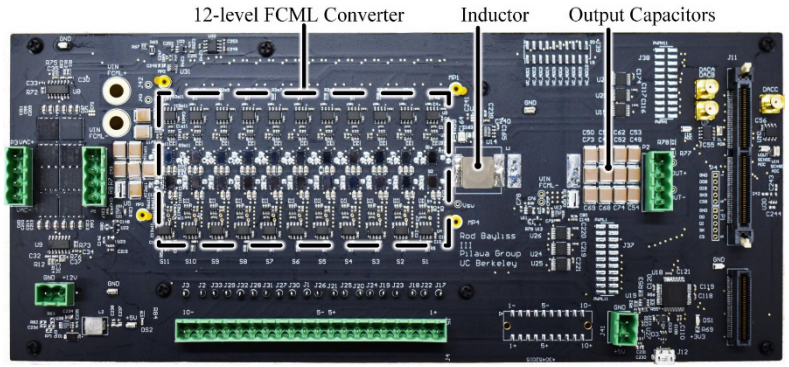
Motivation and Application

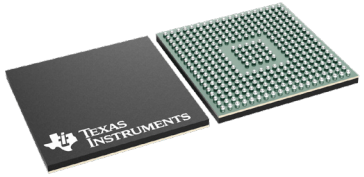
Data center power consumption 1%+ of global electricity demand and growing [1]

Single-stage rectification
- Increased efficiency
- Greater power density



Hardware

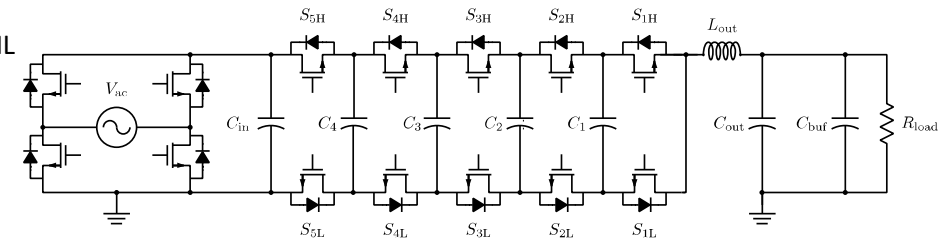




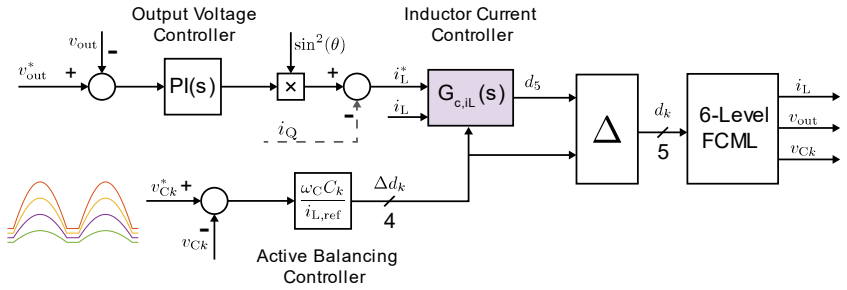
TI C2000 DSP (F28379D)

FCML and Active Flying Capacitor Voltage Balancing

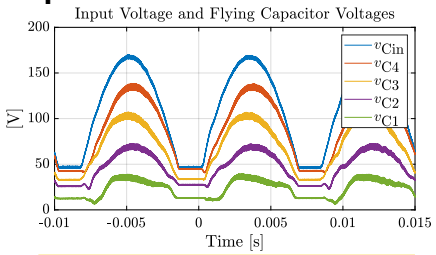
6-Level Buck-Type FCML PFC Rectifier
- Reduced magnetics volume
- High FOM switches

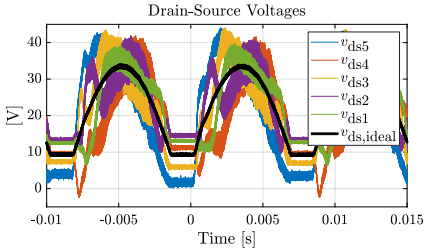


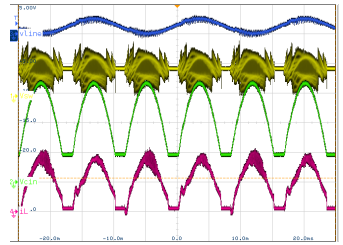
Control Schematic



Experimental Verification







Power Factor	
Target	0.97
Passive Balancing	0.88
Active Balancing	**0.97+**

- Switch voltage stress limited → low voltage switches

References:
[1] N. Jones, "The Information Factories," Nature 2018

Rod Bayliss III Email: rodbay@berkeley.edu

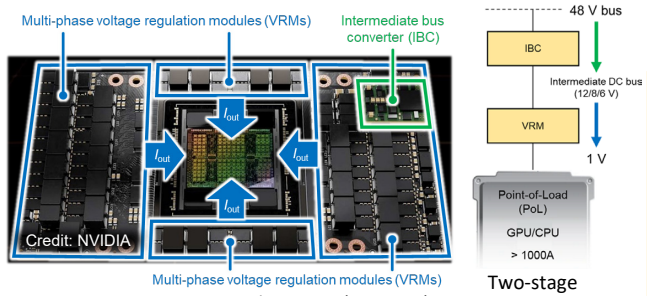
A 1200-A/48-V-to-1-V Switching Bus Converter: Toward Single-Stage Vertical Power Delivery for Next-Generation Ultra-High-Power Microprocessors

Berkeley Power and Energy Center

Background and Motivation

Existing two-stage lateral power delivery (LPD) architecture

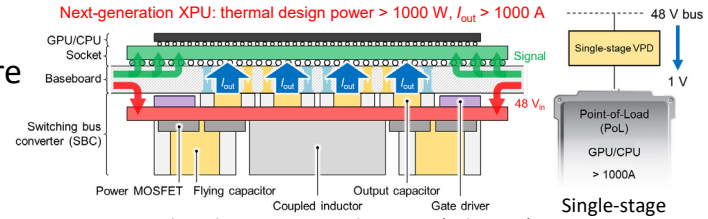
- Large power distribution network (PDN) and high PDN losses
- Occupies a large area on the top side of the baseboard



Existing two-stage LPD architecture (top view)

Proposed single-stage vertical power delivery (VPD) architecture

- Much lower PDN losses
- Saves the topside area for high-speed communication and memories



Proposed single-stage VPD architecture (side view)

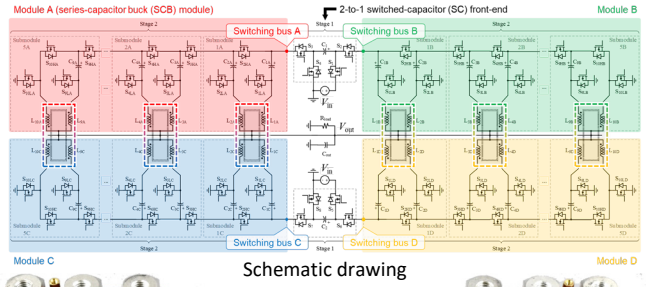
Proposed Switching Bus Converter (SBC)

Hybrid switched-capacitor topology

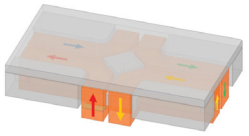
- Two 2-to-1 switched-capacitor (SC) front-ends
- Four series-capacitor buck (SCB) modules
- Two switching buses

Hardware prototype

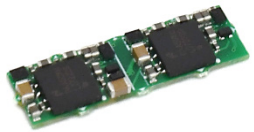
- Good modularity
- Custom four-phase coupled inductor
- Efficient and compact gate drive circuitry



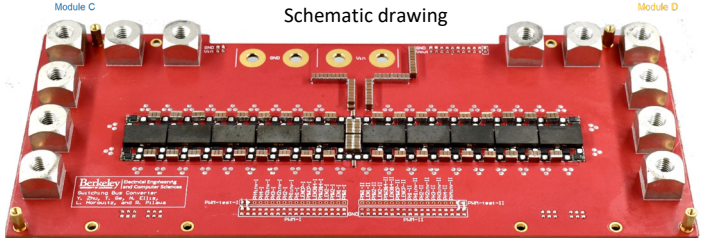
Schematic drawing



Four-phase coupled inductor



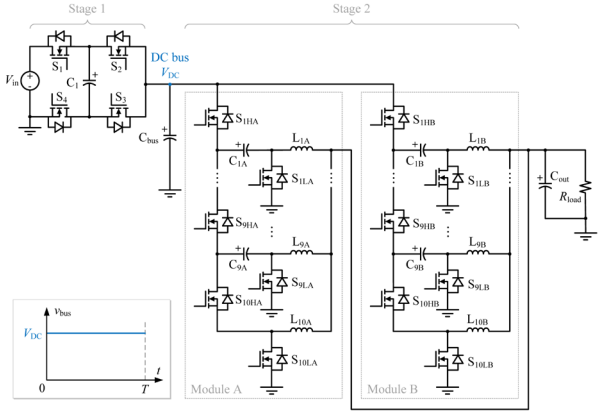
Gate drive daughterboard



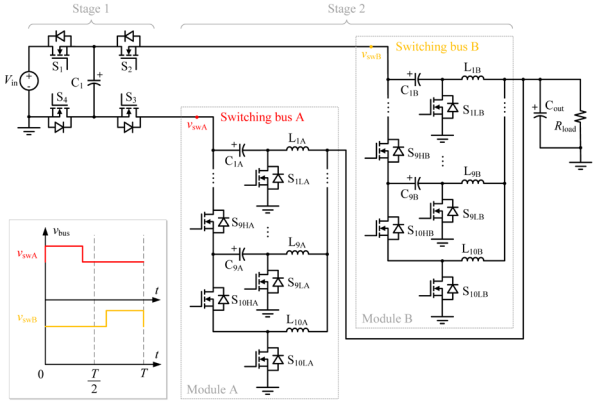
Photograph of the hardware prototype

Advantages of Switching-Bus-Based Architecture

- Does not require a large decoupling capacitor to maintain a stiff DC bus voltage
- One redundant switch can be removed on each switching bus while two stages are merged
- Ensures complete soft-charging operation



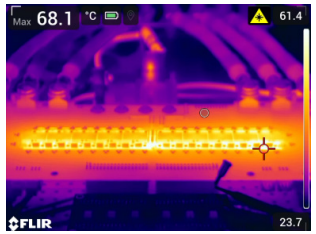
DC-bus-based architecture



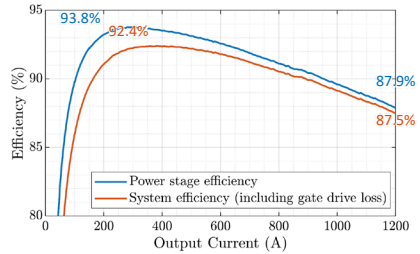
Switching-bus-based architecture

Experimental Results and Performance Comparison

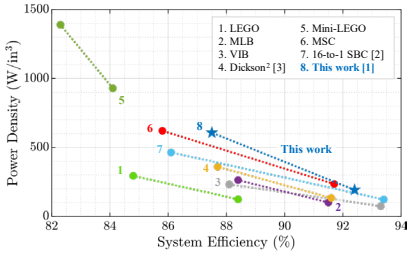
- 92.4% peak system efficiency and 607 W/in^3 power density (including gate drive loss and volume)



Thermal image at equilibrium with 220 CFM air cooling (I_{out}=1200 A)



Measured 48-V-to-1-V efficiency



Performance comparison between this work and the state-of-the-art 48-V-to-1-V hybrid SC works

References:

[1] Y. Zhu , et al., "A 48-V-to-1-V Switching Bus Converter for Ultra-High-Current Applications," COMPEL 2023. **[Best Paper Award]**
[2] Y. Zhu , et al., "A 500-A/48-to-1-V Switching Bus Converter: A Hybrid Switched-Capacitor Voltage Regulator with 94.7% Peak Efficiency and 464-W/in3 Power Density," APEC 2023.
[3] Y. Zhu , et al., "A Dickson-Squared Hybrid Switched-Capacitor Converter for Direct 48 V to Point-of-Load Conversion," APEC 2022.

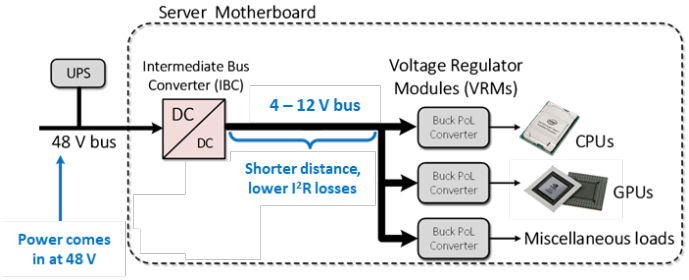
Yicheng Zhu, Ting Ge, Nathan M. Ellis, and Jiarui Zou Email: {yczhu, gting, nathanmilesellis, jiarui.zou}@berkeley.edu

48-to-6 V Cascaded Series-Parallel Converter for Intermediate Bus Applications

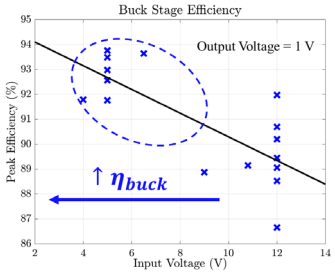
Berkeley Power and Energy Center

Motivation and Application

Data center power delivery has recently moved to a 48 V bus, which must be stepped down at the server racks. Commonly, this bus is stepped down to a 12 V intermediate bus, which is then converted to the low voltage, high current rails needed at the point-of-load (PoL). However, **lower (i.e. 4-8 V) intermediate bus voltages have shown promise in increasing overall system efficiency** by allowing the 2nd stage PoL converter to operate at lower input voltages, and therefore higher efficiency.



48 V Datacenter Two-Stage Architecture



1 V PoL Converter Efficiency

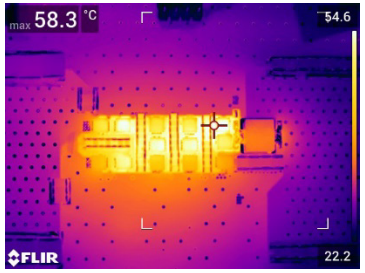
Experimental Validation

The hardware prototype was designed using 25 V and 40 V Si MOSFETs (Infineon OptiMOS) and Class II ceramic capacitors. The inductor is recessed into the PCB to obtain a more power dense design.

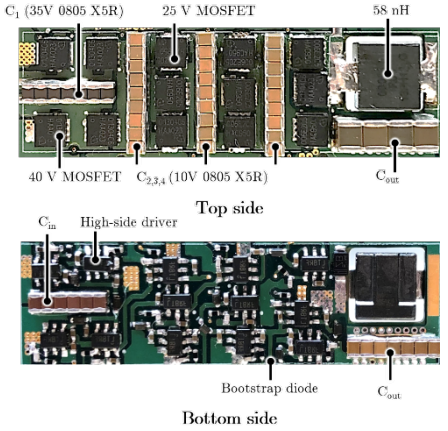
Operating Parameters

	Nominal	Range
V_{in}	48 V	40 – 60 V
V_{out}	6 V	5 – 7.5 V
$I_{out,max}$	70 A	70 A
P_{out}	400 W	330 – 500 W
f_{sw}	50 kHz	50 – 55 kHz

Thermal Photo at I_{out} = 70 A



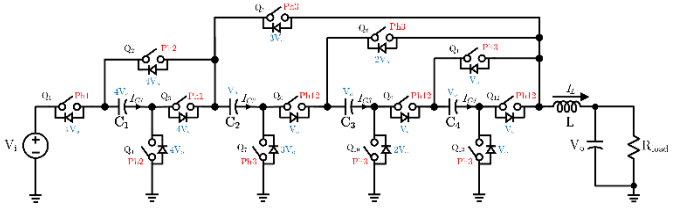
The converter was able to maintain a temperature below 60˚C at the full load current of 70 A with only fan cooling.



Dimensions: 1.76 x 0.51 x 0.21 in (44.7 x 13.0 x 5.3 mm)

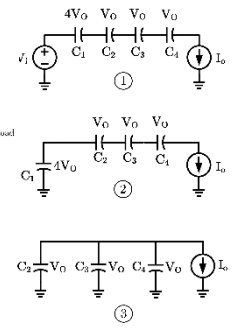
Theory of Operation

The 8:1 cascaded series-parallel (CaSP) converter consists of a 2:1 input stage merged with a 4:1 series-parallel converter. The multi-operating-phase operation allows the converter to achieve a high conversion ratio with fewer components compared to conventional two-phase hybrid switched capacitor circuits. The converter is operated above resonance to reduce RMS currents and make it less sensitive to capacitor tolerance variations.

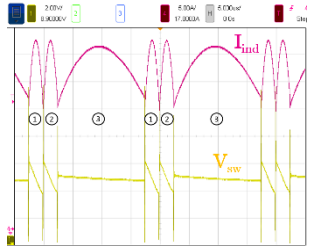


Schematic of 8:1 CaSP Converter

Phase Equivalent Circuits



Operating Waveforms

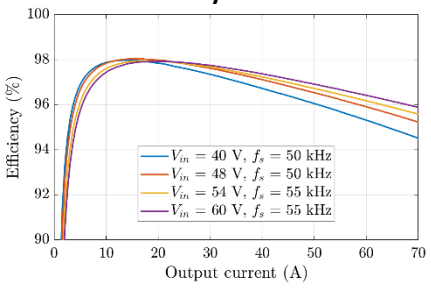


The inductor current does not ripple all the way down to 0 A, owing to the above resonance operation.

References:
[1] R. A. Abramson, Z. Ye, T. Ge and R. C. N. Pilawa-Podgurski, "A High Performance 48-to-6 V Multi-Resonant Cascaded Series-Parallel (CaSP) Switched-Capacitor Converter," *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Phoenix, AZ, USA, 2021.

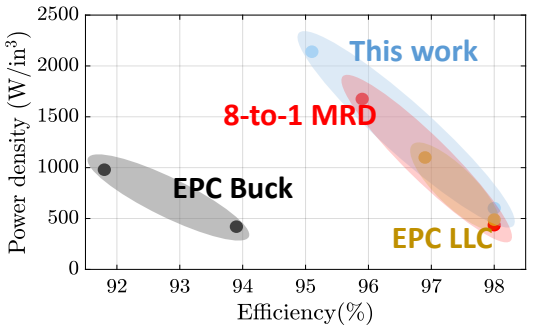
Converter Performance

Efficiency vs. Load



V_{in}	Peak Eff. (%)	Full Load Eff. (%)
40 V	98.0%	94.6%
48 V	98.1%	95.3%
54 V	98.0%	95.7%
60 V	97.9%	96.0%

Comparison with Contemporary State of the Art



Each converter efficiency and power density is plotted at two points:

1) *Peak efficiency load*
2) *Full load*

Owing to the high overall efficiency, the converter exhibits an output droop of 292 mV (or 4.9% of V_{out}), corresponding to an output impedance of 4.2 mΩ.

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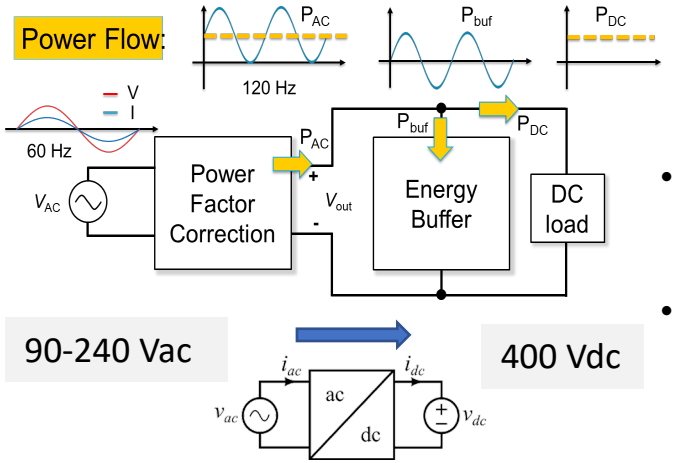
A Bidirectional Liquid-Cooled GaN-based AC/DC Flying Capacitor Multi-Level (FCML) Converter with Integrated Startup and Additively Manufactured Cold-Plate for Electric Vehicle Charging

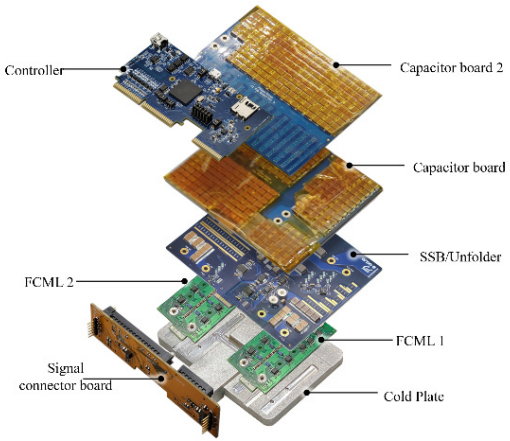
Berkeley Power and Energy Center

Motivation and Application

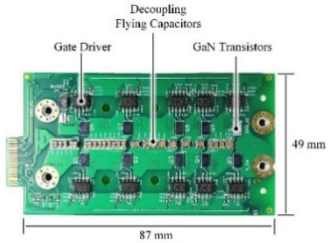


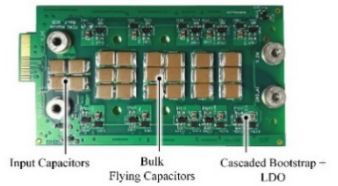
- 90-240 Vac to 400 Vdc is a critical conversion stage for applications such as data center power delivery, electric vehicle charging, etc.
- Ac-dc power factor correction
  - Reduce boost inductor size
- Twice-line frequency power ripple buffering
  - Reduce buffer capacitor size

Hardware Implementation



Modular stack-up of full system





Flying capacitor multi-level"(FCML) converter as the power factor correction stage

- Use of flying capacitors as energy storage greatly decreases volume of passive components and reduce filtering needs

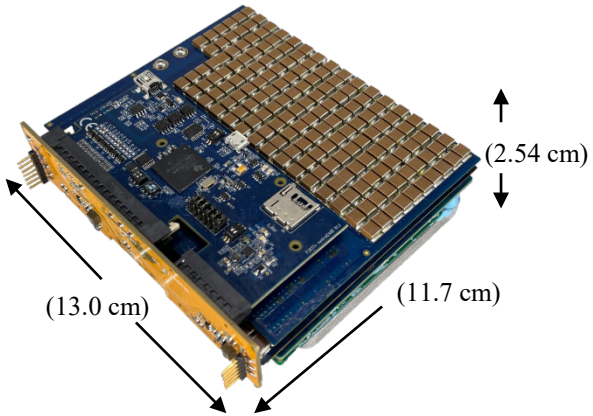
Series-stacked Buffer as energy buffer stage

- Use of active circuitry decreases capacitance requirement for twice-line frequency buffering and further promoted volume reduction

Design Objectives

High Power Density

Reduce system volume via new circuit topologies and control

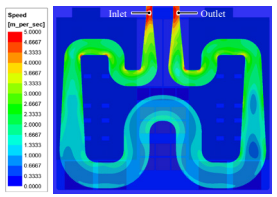


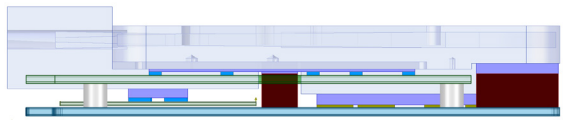
Reduced Weight

Custom 3D-printed cold-plate (collaboration with Miljkovic Group at UIUC)

3D printed cold-plate

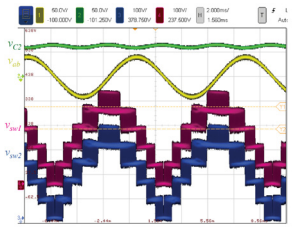
Printed Fluid Channels



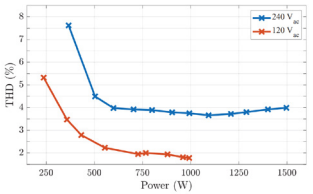


Experimental Verification

Parameter	Notes
Peak tested power	6.1 kW
Peak efficiency (1.1 kW)	99.1%
Efficiency @ 6.1 kW	97.8%
PFC up to 1.5 kW	> 99.6%
Box-volume power density **with** cold plate:	7.6 kW/L



400 V_{dc} to 240 V_{ac} system waveforms at 6.1 kW



THD up to 1.5 kW

Kelly Fernandez, Rahul Iyer, Jiarui Zou Email: kefernandez@berkeley.edu, rkiyer@berkeley.edu, Jiarui.zou@berkeley.edu

References:
[1] D. Chou et al., "An Interleaved 6-Level GaN Bidirectional Converter with an Active Energy Buffer for Level II Electric Vehicle Charging," 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), Phoenix, AZ, USA, 2021
[2] Z. Liao, D. Chou, K. Fernandez, Y. -L. Syu and R. C. N. Pilawa-Podgurski, "Architecture and Control of An Interleaved 6-Level Bidirectional Converter With an Active Energy Buffer for Level-II Electric Vehicle Charging," 2020 IEEE Energy Conversion Congress and Exposition (ECCE),
[3] K. Fernandez et al., "A Bidirectional Liquid-Cooled GaN-based AC/DC Flying Capacitor Multi-Level Converter with Integrated Startup and Additively Manufactured Cold-Plate for Electric Vehicle Charging," 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), Houston, TX, USA, 2022

An EMI-Compliant and Automotive-Rated 48 V-to-PoL Dickson-Based Hybrid Switched Capacitor DC-DC Converter

Berkeley Power and Energy Center

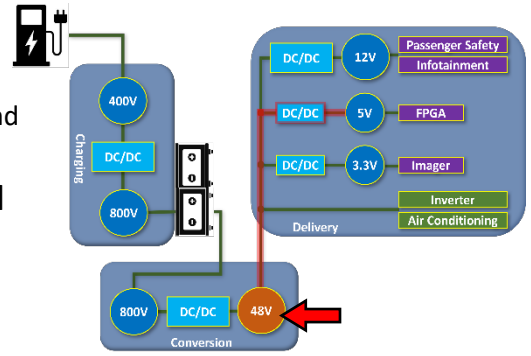
Motivation and Application

Data center power delivery and automotive powertrains tending towards a 48 V distribution rail

- Higher intermediate bus voltages minimize losses and reduce cabling weight

This work demonstrates the merit of hybrid SC topologies for use in 48 V automotive systems

- Regulating Dickson-based hybrid SC topology
- EMI mitigation techniques – filtering and spread-spectrum frequency modulation



48 V automotive bus architecture

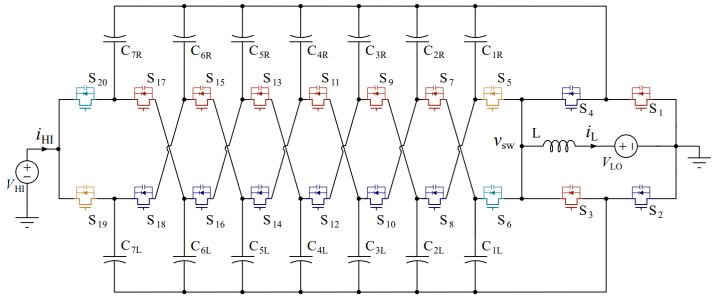
Topology and Challenges

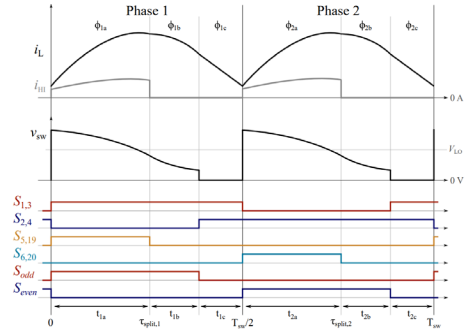
Hybrid switched-capacitor, 8-to-1 interleaved-input, single-inductor Dickson converter

- Differential input → continuous input current → reduced required input filter
- Inductor at output → filtering and EMI shielding at low side
- Inductor at output → voltage regulation

Challenges

- Split-phase switching necessary for soft-charging of the flying capacitors
- Automotive component selection
- High efficiency, power density, and CISPR 25 Class 5 EMI compliance



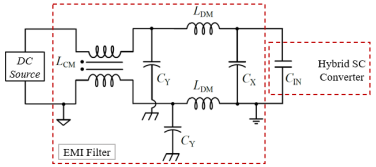


Hardware Implementation

Uses only automotive-qualified parts

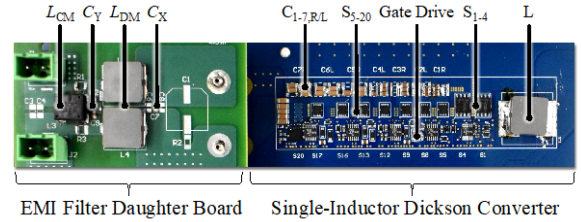
Switch selection based on required function, both Si and GaN

EMI input filter and spread spectrum frequency modulation (SSFM) to reduce EMI



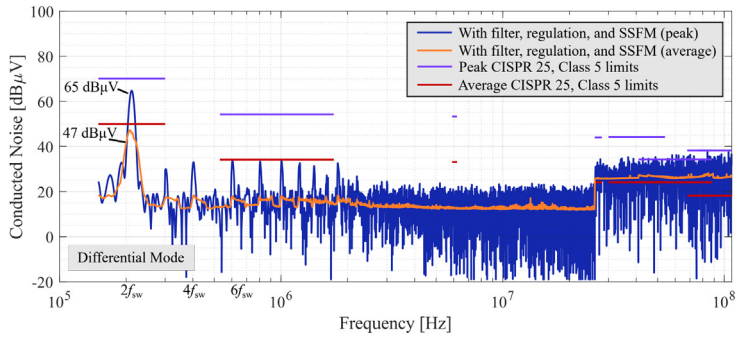
Input EMI filter schematic

Switches and Key Parameters			
Switch	**S1-S4**	**S5-S18**	**S19-S20**
Tech	Si	Si	GaN
Function	Bridge switches	'String' switches	Input switches
$R_{DS(on)}$	1.4 mΩ	3.5 mΩ	2.5 mΩ
V_{DS}	40 V	40 V	80 V



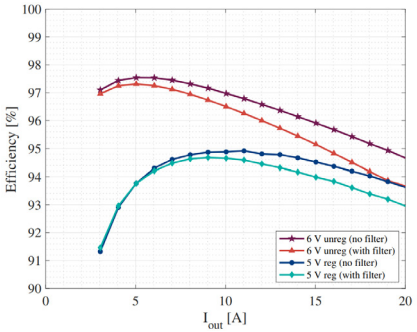
Experimental Results

Differential Mode (DM) EMI results



Peak and average DM emissions plots for above-resonant (~106 kHz) regulated 5 V operation with SSFM enabled

Converter Operating Parameters			
V_{IN}	**V_{OUT}**	**$P_{LO,max}$**	**f_{sw}**
48 V	6 V, 5 V	120 W	106 kHz



Measured efficiency of hardware prototype

References: [1] M. E. Blackwell, et al., "Direct 48 V to 6 V Automotive Hybrid Switched-Capacitor Converter with Reduced Conducted EMI," *2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL)*. [2] S. Krishnan, et al., "An EMI-Compliant and Automotive-Rated 48V to Point-of-Load Dickson-Based Hybrid Switched-Capacitor DC-DC Converter," *2023 IEEE Transportation Electrification Conference & Expo (ITEC)*

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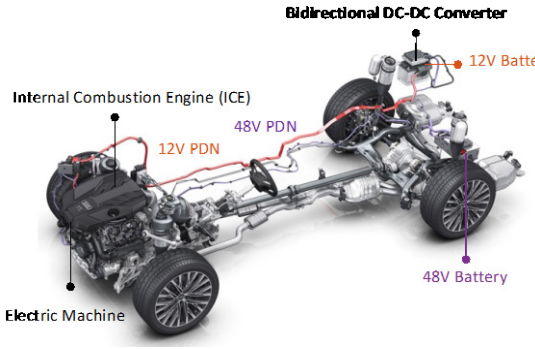
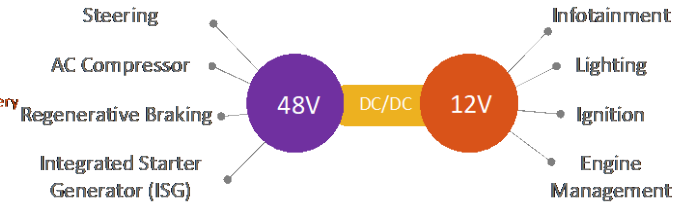
Bidirectional Power Transfer in Hybrid Switched-Capacitor Converter for 48V/12V Regulated Automotive Applications

Berkeley Power and Energy Center

Motivation and Application



Dual Battery System in
Mild Hybrid Electric Vehicle (MHEV)
(Source: Audi A8 Powertrain)



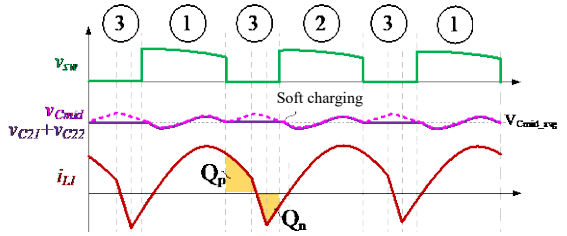
Need:

- 48V battery should be able to deliver **extra power** to 12V battery based on increased load demand and vice-versa.

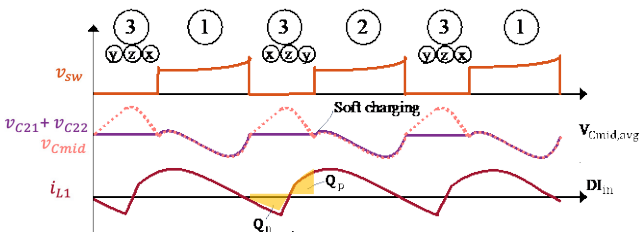
Challenges:

- Delivery of **high current** with **high efficiency** and **high power density in both directions**

Advantages of Proposed Control Technique



48V to 12V Conversion

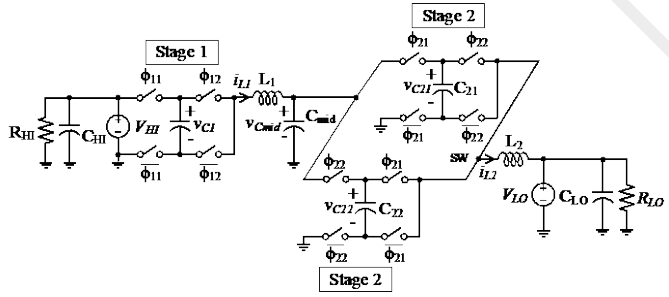


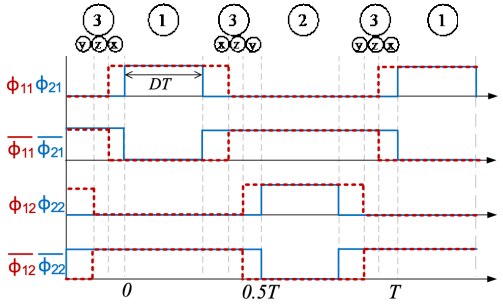
12V to 48V Conversion

- Implements Natural Balancing of all flying capacitors.
- Achieves Soft-charging and soft-switching .
- Minimizes the size of the intermediate capacitor C_{mid}.

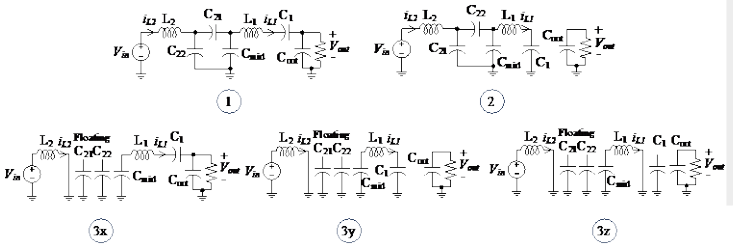
Converter Topology

- 48V-to-12V **regulated** cascaded hybrid resonant-PWM converter [1]
- 1st stage uses a conventional doubler in resonant mode
- 2nd stage used two interleaved doublers operating in PWM mode.





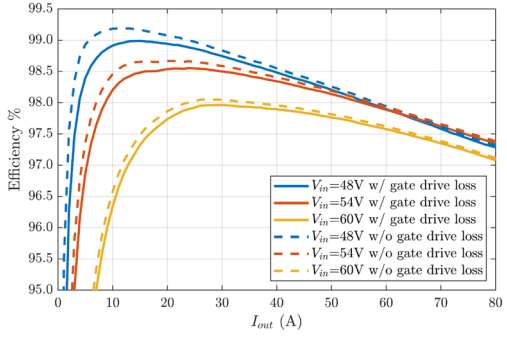
Resonant (Stage-1) + PWM (Stage-2) Operation

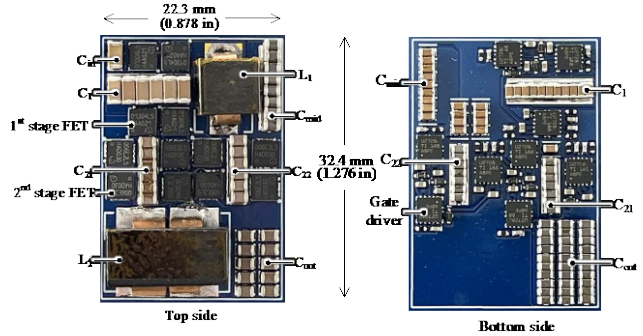


Hardware Demonstration and Results

Measured Efficiency at:

- Input voltage: 48 – 60V
- 80 A full-load current
- Regulated 12 V output





- 80A, 99% peak eff. 3115 W/in^3 power density
- 21% loss and 63% size reduction over SOTA

[1] T. Ge, et. al., "A Regulated Cascaded Hybrid Switched-Capacitor Converter with Soft-Charging and Zero Voltage Switching for 48-to-12-V," 2023 IEEE APEC.

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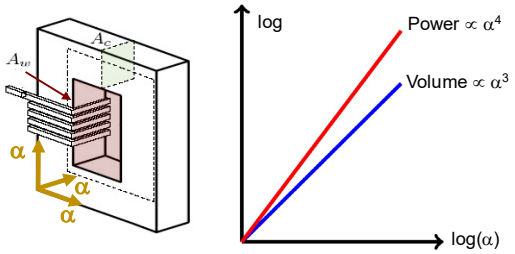
Converter Topologies and Control Strategies Leveraging Piezoelectrics for High-Performance Miniaturized Power Conversion

Berkeley Power and Energy Center

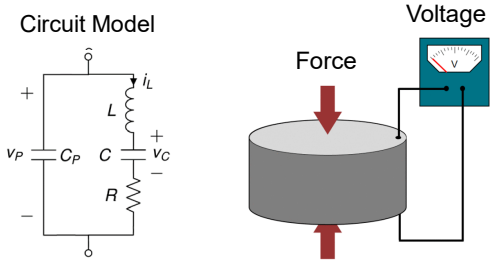
Piezoelectrics as Passive Components

Magnetics present fundamental size and performance challenges at small scales



Piezoelectrics are promising alternative passives for miniaturized power conversion

Piezoelectrics store energy in mechanical compliance and inertia

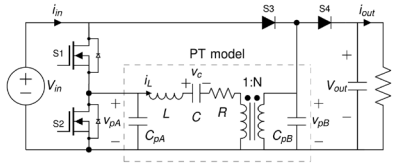


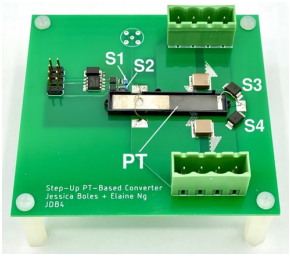
- ✓ High power density
- ✓ High efficiency
- ✓ Isolation
- ✓ Planar form factor
- ✓ Batch fabrication
- ✓ Integration potential

Converter Topologies Based on Piezoelectrics

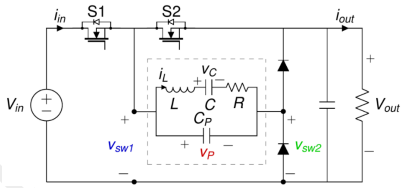
We develop converter topologies that leverage the advantages of piezoelectrics in a variety of applications

Piezoelectric-transformer-based dc-dc converter

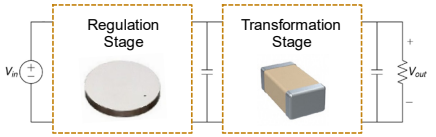




Piezoelectric-resonator-based dc-dc converter



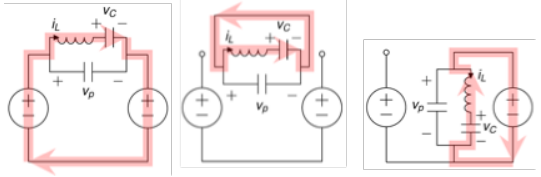
Hybrid piezo / switched capacitor converter



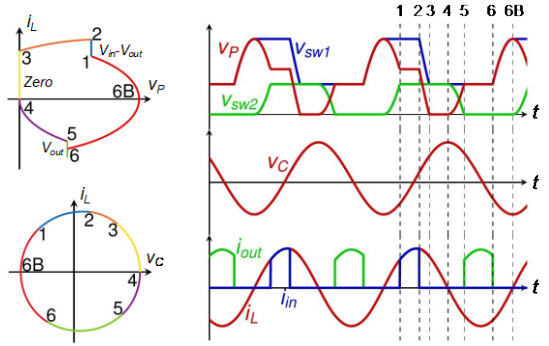
Control for Efficient Utilization of Piezoelectrics

We develop high-performance switching sequences and control strategies tailored to optimal utilization of piezoelectrics

Six-stage sequence fixed voltage states

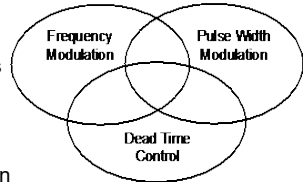


Six-stage sequence state trajectories and waveforms



High-Efficiency Behaviors:
- Soft charging of *Cp*
- Soft switching of all switches
- Minimal charge circulation

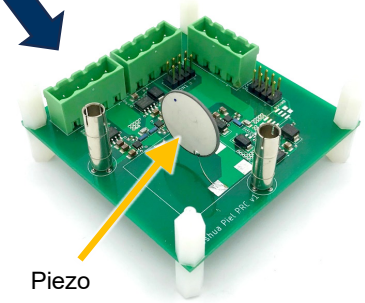
Practical Characteristics:
- Wide voltage gain range
- Simple switch implementation



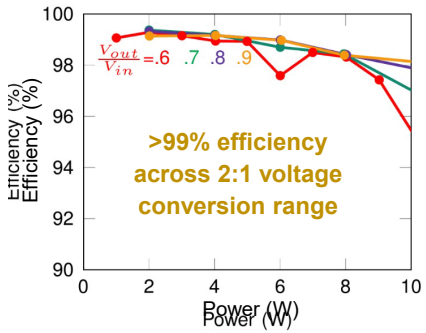
Experimental Demonstration

We experimentally demonstrate the high performance capabilities of piezoelectric-based power conversion

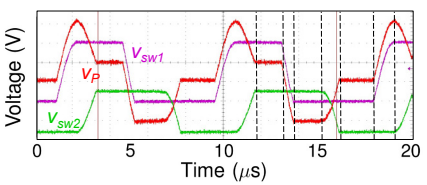
PR-based dc-dc converter



Varied Gain, V_{in} =100 V



V_{in} = 100 V, V_{out} = 40 V, P_{out} = 6 W



J. D. Boles et al., "Enumeration and analysis of dc-dc converter implementations based on piezoelectric resonators," *IEEE TPEL*, 2021.
J. D. Boles et al., "A piezoelectric-resonator-based dc-dc converter demonstrating 1 kW/cm³ resonator power density," *IEEE TPEL*, 2023.
J. D. Boles et al., "Piezoelectric-based power conversion: recent progress, opportunities, and challenges,," *IEEE CICC*, 2022.

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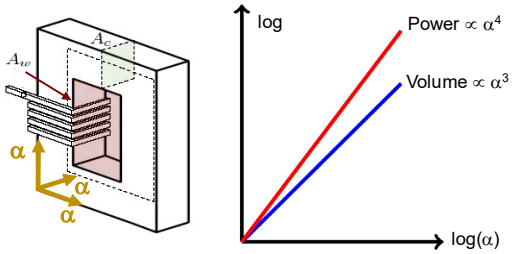
Piezoelectric Passive Components for High-Performance Miniaturized Power Conversion

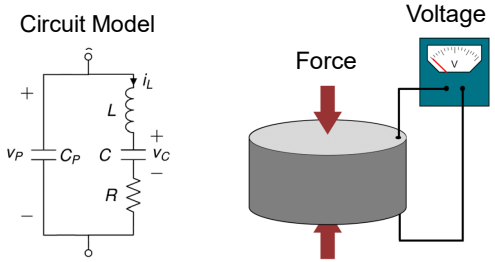
Berkeley Power and Energy Center

Piezoelectrics as Passive Components

Magnetics present fundamental size and performance challenges at small scales



Piezoelectrics store energy in mechanical compliance and inertia

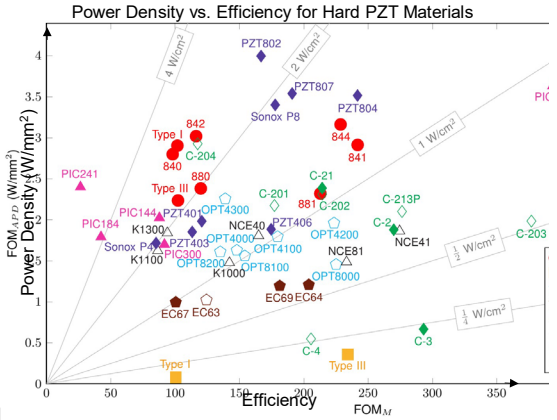


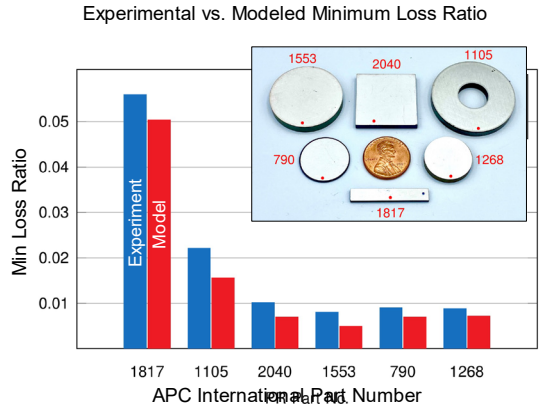
- ✓ High power density
- ✓ High efficiency
- ✓ Isolation
- ✓ Planar form factor
- ✓ Batch fabrication
- ✓ Integration potential

Piezoelectrics are promising alternative passives for miniaturized power conversion

Materials and Vibration Modes

We evaluate the efficiency and power density capabilities of numerous piezoelectric materials and vibration modes

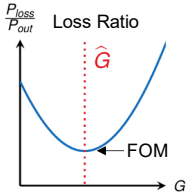


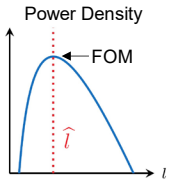


Structures and Design Optimization

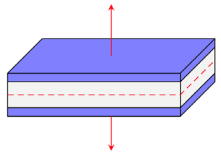
We develop design guidelines for achieving maximum efficiency and power density in a variety of piezoelectric component structures

Geometry optimization

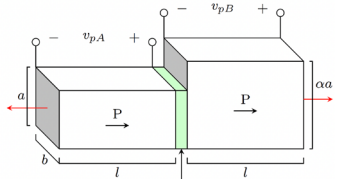




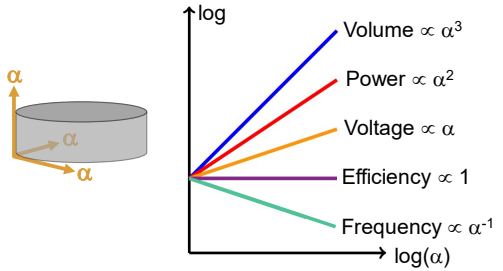
Mass-augmented piezoelectric resonator



Piezoelectric transformer

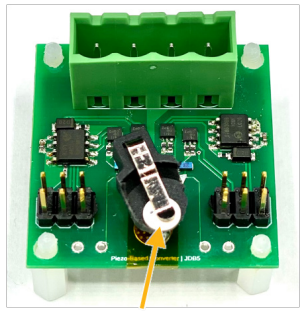


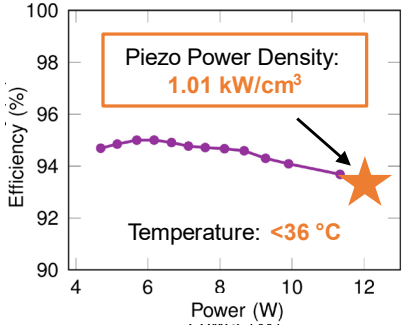
Fundamental scaling laws show that power density *rises* as volume decreases



Experimental Demonstration

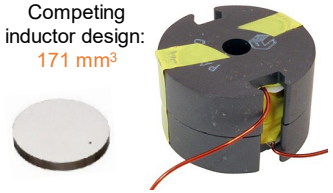
We experimentally demonstrate the drastic miniaturization capabilities of piezoelectrics compared to magnetics





Competing inductor design: 171 mm³

This piezo design: 12 mm³



J. D. Boles et al., "Evaluating Piezoelectric Materials and Vibration Modes for Power Conversion," *IEEE TPEL*, 2022.
J. D. Boles et al., "A piezoelectric-resonator-based dc-dc converter demonstrating 1 kW/cm³ resonator power density," *IEEE TPEL*, 2023.
J. D. Boles et al., "Piezoelectric-based power conversion: recent progress, opportunities, and challenges,," *IEEE CICC*, 2022.

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A General Approach for Design Optimization of High-Performance Hybrid Switched-Capacitor Converters

Berkeley Power and Energy Center

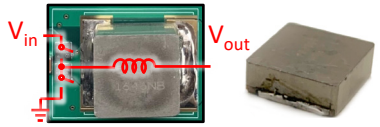
Motivation and Application

Hybrid switched-capacitor converters

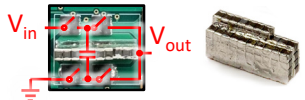
- More capacitive energy storage than inductive energy storage for size reduction
- Multiple low-voltage switches in place of a single high-voltage switch for efficiency improvement

Topology Comparison

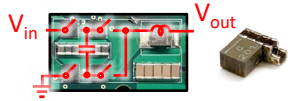
- Analytical method to compare relative size and performance of various topologies
- Include the impacts of capacitor voltage ripple and inductor current ripple on passive component volume and switch stress



Buck: 2059 mm^3
97% peak eff.

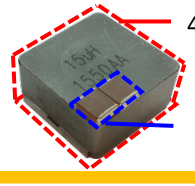


Pure SC: 272 mm^3
99% peak eff.



Hybrid SC: 76 mm^3
99% peak eff.

Performance comparison at 48V-to-24 V

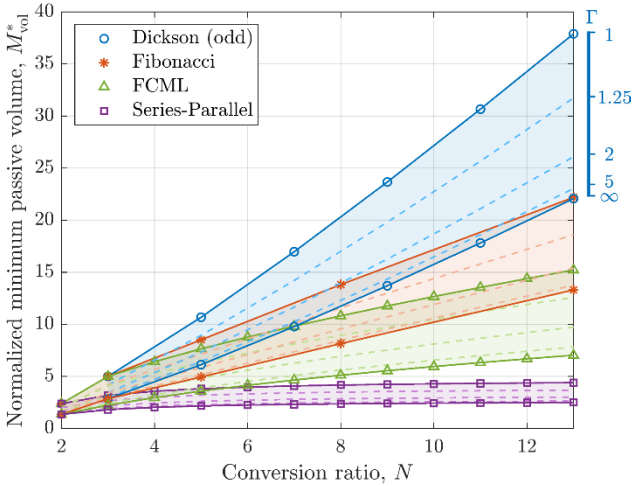


4 mJ of inductive energy storage

80 mJ of capacitive energy storage (after dc-derating)

Impacts of Switching Frequency and Conversion Ratio on Minimal Passive Volume [1]

- Series-Parallel has smaller passive volume → Higher power density
- Increasing $\Gamma = \frac{f_{sw}}{f_{res}}$ → smaller passive volume → Higher power density



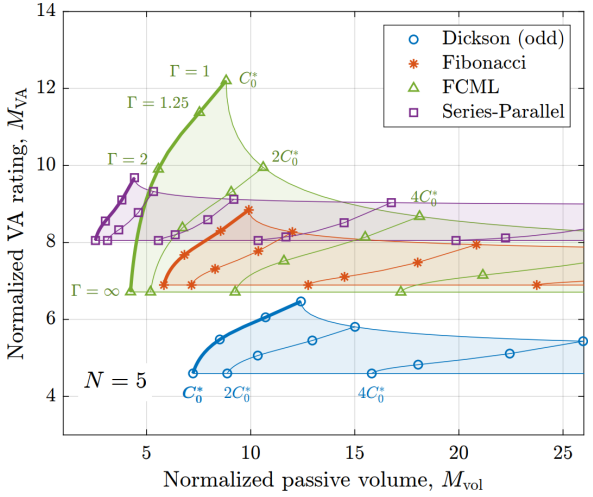
Passive Component Volume and Switch Stress Trade-Off

Increasing the switching frequency beyond resonance

- Trading ↑ switching loss for ↓ conduction loss

Increasing capacitance beyond minimal volume

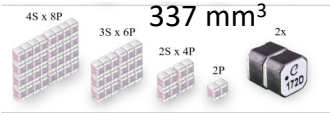
- Trading ↑ volume for ↓ VA rating (efficiency)



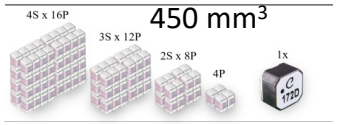
Validation of Analytical Model

$\rho_C = 8800\ \mathrm{J/m^3}$ $\rho_L = 123\ \mathrm{J/m^3}$

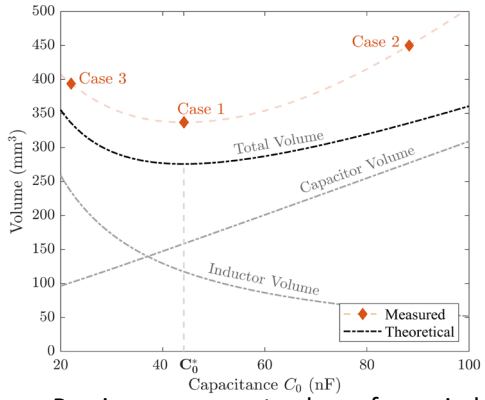
Case 1 — 337 mm^3



Case 2 — 450 mm^3



Case 3 — 394 mm^3



Passive component volume for varied capacitance to validate minimal volume method

References:
[1] N. M. Ellis, et. al., "A General Analysis of Resonant Switched Capacitor Converters Using Peak Energy Storage and Switch Stress Including Ripple," in *IEEE Transactions on Power Electronics, Early Access.*
[2] J. Azurza Anderson, G. Zulauf, J. W. Kolar and G. Deboy, "New Figure-of-Merit Combining Semiconductor and Multi-Level Converter Properties," OJPEL 2020.

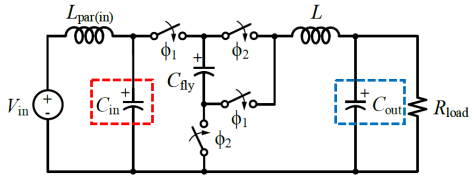
Dr. Nathan Ellis, Maggie Blackwell, Rose Abramson, Dr. Nathan Brooks*, Dr. Sam Coday*
Email: {nathanmilesellis, blackwell, rose_abramson} @berkeley.edu

Modeling and Control of Pure and Resonant Switched-Capacitor Converters with Finite Terminal Capacitances

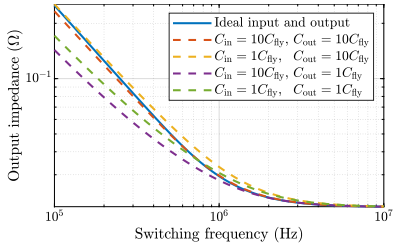
Berkeley Power and Energy Center

Background and Motivation

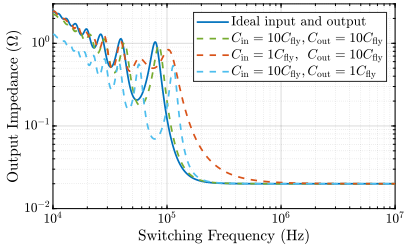
- Insufficient terminal capacitances can greatly affect converter efficiency
- Bulky terminal capacitors become the bottleneck of converter miniaturization



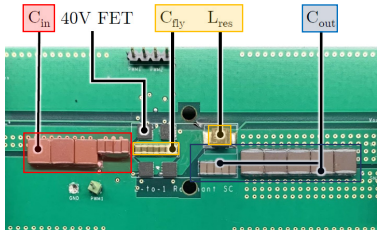
(a) Schematic



Output impedance of a 2-to-1 pure SC converter with different C_{in} and C_{out}



Output impedance of a 2-to-1 resonant SC converter with different C_{in} and C_{out}



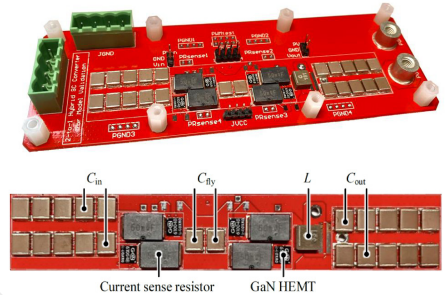
(b) Hardware prototype
2-to-1 resonant SC (ReSC) converter

Simulation and Experimental Verification

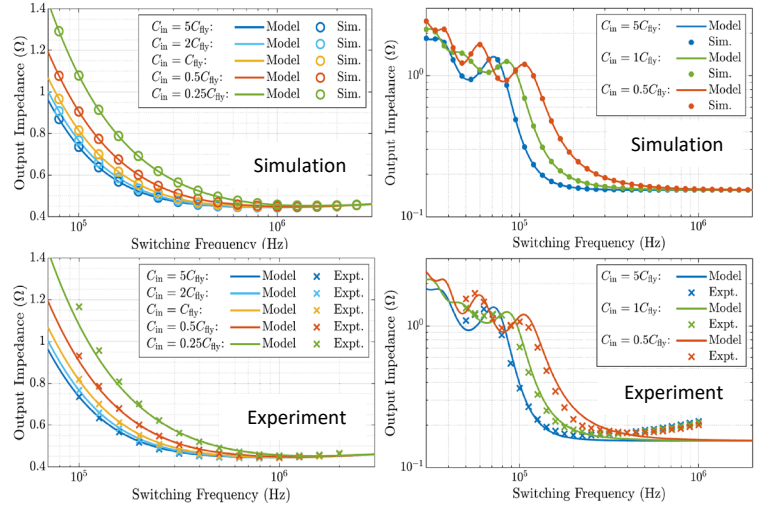
Key considerations

- Minimize switching loss
- Accurate parameter acquisition

High accuracy

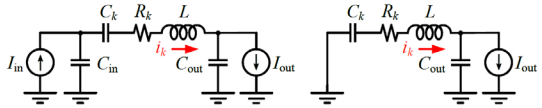


Hardware prototype



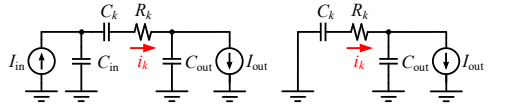
Modeling Derivation and Effect Analysis

Simplified circuit model and general output impedance model



(a) Phase 1 (b) Phase 2

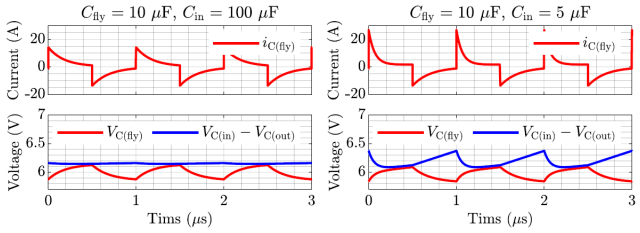
Circuit model of a ReSC converter with C_{in} and C_{out}



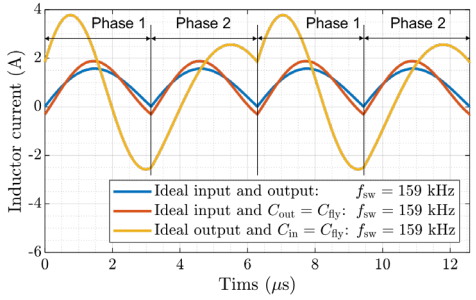
(a) Phase 1 (b) Phase 2

Circuit model of a pure SC converter with C_{in} and C_{out}

Effect of terminal capacitances



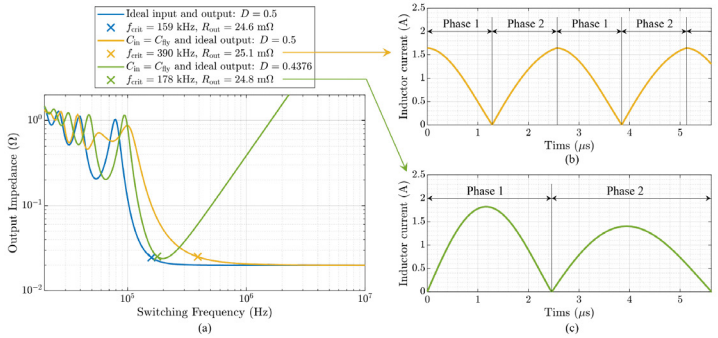
Inductor current waveform of a 2-to-1 pure SC converter with different terminal capacitances



Inductor current waveform of a 2-to-1 ReSC converter with different terminal capacitances

Multi-Resonant Compensation Control (MRCC)

- Challenge: zero current switching (ZCS) is not achievable with 0.5 duty ratio with small C_{in}
- Solution: ensure ZCS operation with the optimal duty ratio and switching frequency
- Result: 5x terminal capacitance reduction without harming efficiency



(a) Comparison of output impedance. (b) Inductor current waveform of the conventional control. (c) Inductor current waveform of MRCC.

References:

[1] Y. Zhu *et al.*, "Modeling and Analysis of Resonant Switched-Capacitor Converters with Finite Terminal Capacitances," COMPEL 2021.

[2] Y. Zhu *et al.*, "Multi-Resonant Compensation Control for Terminal Capacitance Reduction in Resonant Switched-Capacitor Converters," COMPEL 2021.

[3] Y. Zhu *et al.*, "Modeling and Analysis of Switched-Capacitor Converters with Finite Terminal Capacitances," APEC 2021.

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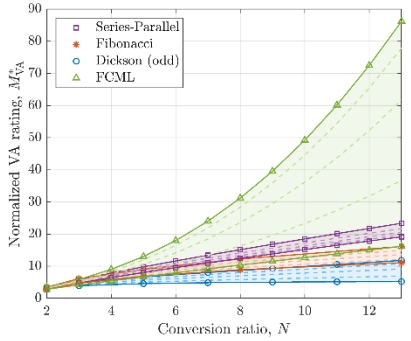
Analysis of Phase Timings for a Zero-Voltage Switching, Split-Phase Hybrid Dickson Converter

Berkeley Power and Energy Center

Motivation and Application

- Dickson-based converters are popular for hybrid switched capacitor (SC) solutions due to the reduced switch stress as compared to other topologies [1]
- Applications: high-conversion ratio systems
  - 48 V bus architectures for data centers and automotive powertrains
- Transistor switching losses can be significant share of overall losses, especially with trends towards faster switching frequencies
- Soft-switching techniques, such as zero-current and zero-voltage switching (ZCS and ZVS) can be used to reduce these losses

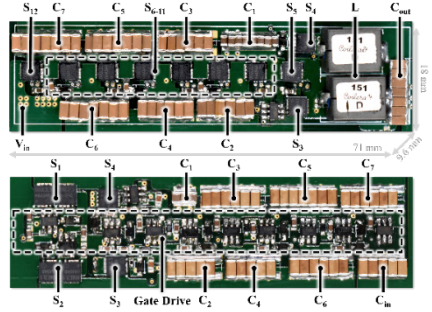


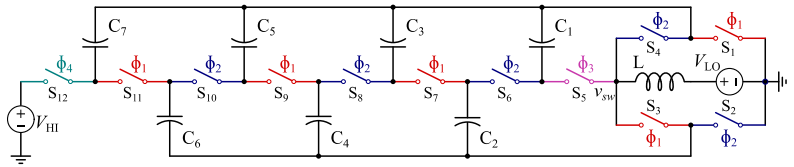
Switch Stress Metric (VA rating) for various hybrid SC converters over conversion ratios showing the Dickson converter having very low relative switch stress

Hardware

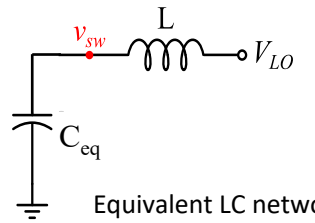
48 V-to-6 V prototype

- Per-phase analysis of an equivalent LC network to determine phase-timings
- Equivalent capacitance Ceq:
  - Main phases: A network of the flying capacitors C_1-C_7
  - ZVS sub-phases: A network of linearized transistor output capacitances [2]





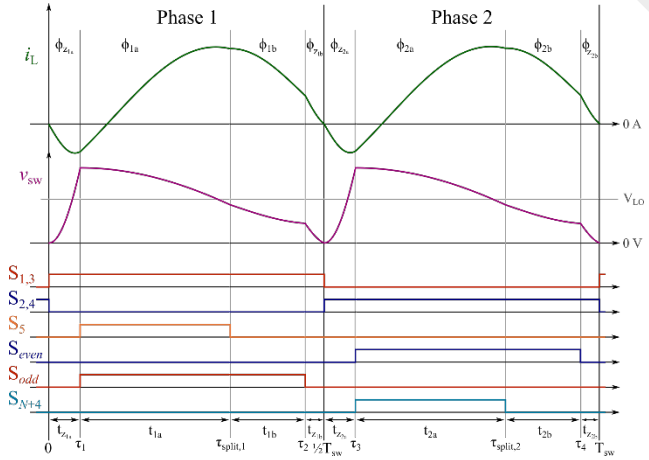
Schematic drawing of the 8-to-1 hybrid Dickson power stage



Equivalent LC network for per-phase analysis

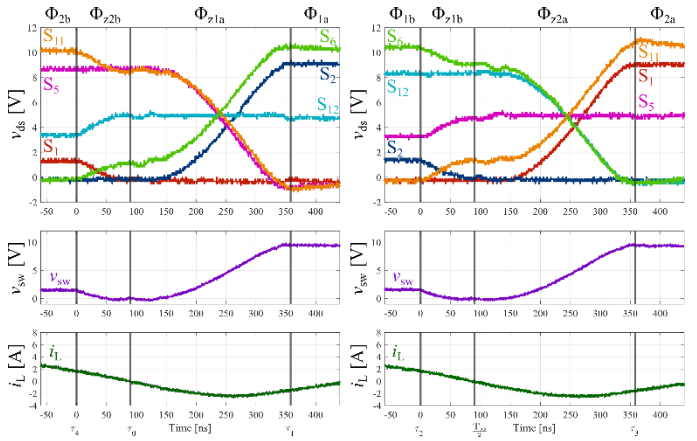
Challenges

- Phase-timings become non-trivial to determine
- ZVS timings are also non-trivial
  - Non-linear switch output capacitance
  - Multiple switches with different blocking voltages

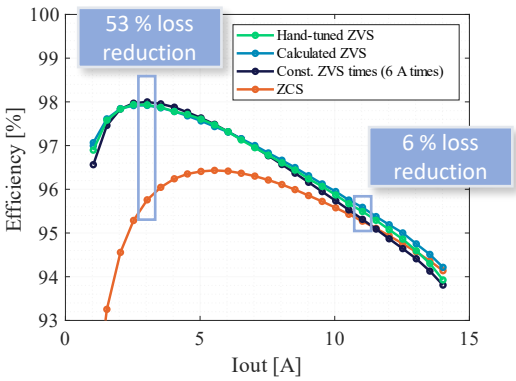


Exemplary phase-timings and waveforms of a resonant Dickson converter achieving ZVS on all switches

Experimental Verification



Measured drain-source voltages showing ZVS for all switches



An efficiency comparison of ZVS to ZCS, as well as calculated timings to fixed timings

References:
[1] N. M. Ellis, et. al., "A General Approach to Optimization and Control of Resonant Switched Capacitor Converters Using Peak Energy Storage and Switch Stress Including Ripple Considerations," *IEEE Transactions on Power Electronics, Early Access*.
[2] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "ZVS of Power MOSFETs Revisited," IEEE Transactions on Power Electronics, vol. 31, no. 12, pp. 8063–8067, Dec 2016.

Maggie Blackwell
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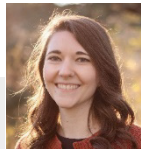
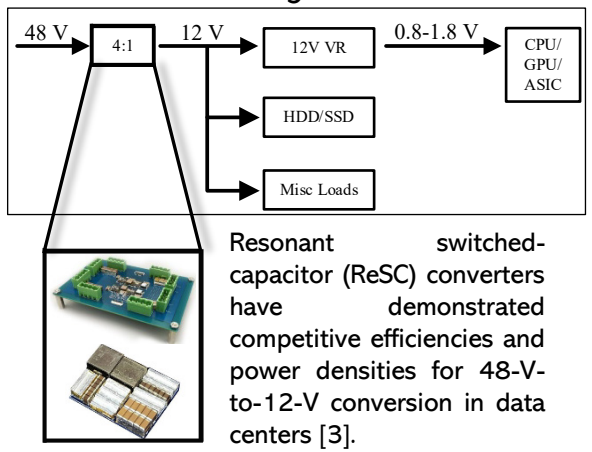


Autotuning of Resonant Switched-Capacitor Converters for Soft Switching Operation

Berkeley Power and Energy Center

Motivation and Application

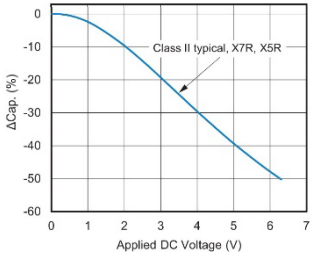
Data Center Two-Stage Power Architecture



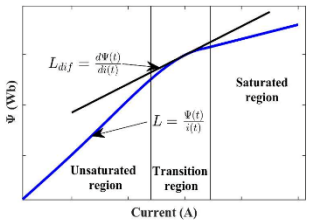
Resonant switched-capacitor (ReSC) converters have demonstrated competitive efficiencies and power densities for 48-V-to-12-V conversion in data centers [3].

Due to finite terminal filtering capacitances, the efficiency of ReSC converters is often maximized when they are precisely soft switched [4]. However, circuit non idealities render ZCS and ZVS timing challenging to estimate creating the need for active control techniques.

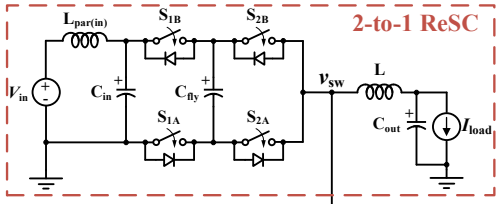
Class II MLCC DC Bias Derating

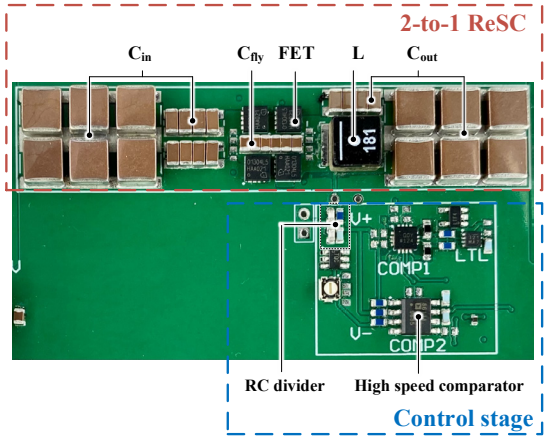


Inductor Soft Saturation



Hardware

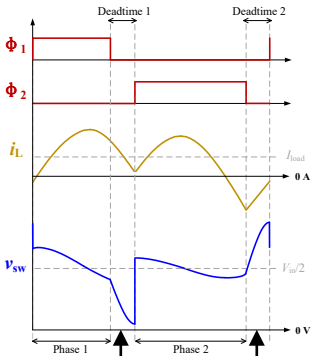




The presented 2-to-1 converter is the foundational ReSC topology. The control technique is verified on a 48-V-to-24-V hardware prototype and can be extended to higher conversion ratio topologies.

Theory and Control

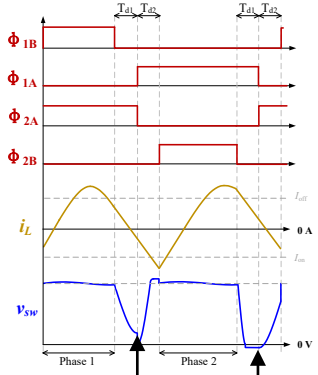
Non-Ideal ZCS



Positive turn-off inductor current → switch node voltage below $\frac{V_{in}}{2}$

Negative turn-off inductor current → switch node voltage above $\frac{V_{in}}{2}$

Non-Ideal ZVS

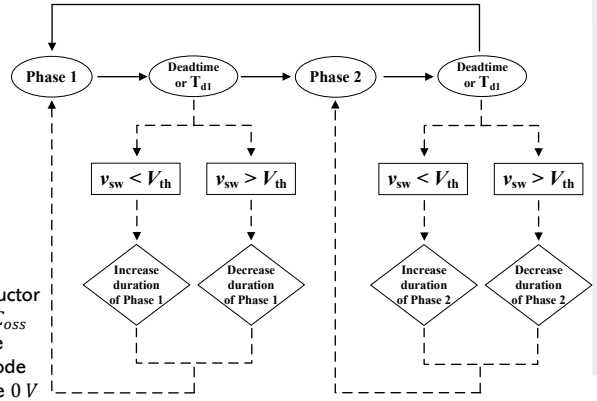


Insufficient inductor current for C_{oss} discharge → switch node voltage above $0\ V$

Excessive inductor current for C_{oss} discharge → switch node voltage above $0\ V$

By sensing the switch node voltage, non-ideal soft switching conditions can be detected. Complete ZCS or ZVS can then be achieved by implementing the proposed control scheme.

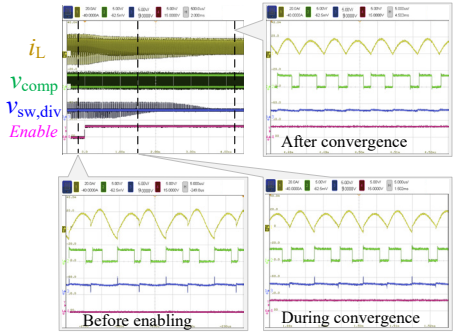
Control Flowchart



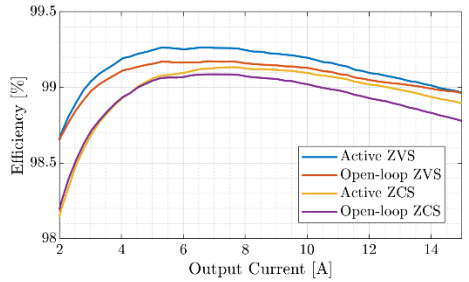
Experimental Verification

- Convergence to complete soft switching can be achieved from a wide range of initial switching frequencies.
- Active ZVS and ZCS control allow for higher peak efficiencies than the conventional open-loop techniques.

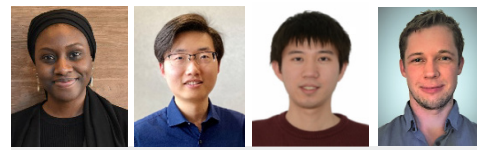
Convergence to Soft Switching



Efficiency



References:
[1] H. Sambo, Y. Zhu, T. Ge, N. Ellis, and R. Pilawa-Podgurski, "Autotuning of Resonant Switched-Capacitor Converters for Zero Current Switching and Terminal Capacitance Reduction," APEC 2023.
[2] H. Sambo, Y. Zhu, and R. Pilawa-Podgurski, "Autotuning of Resonant Switched-Capacitor Converters for Zero Voltage Switching," COMPEL 2023.
[3] T. Ge, Z. Ye, and R. Pilawa-Podgurski, "Geometrical State-Plane Analysis of Resonant Switched-Capacitor Converters: Demonstration on the Cascaded Multiresonant Converter," TPEL 2023.
[4] Y. Zhu, Z. Ye, T. Ge and R. Pilawa-Podgurski, "Multi-Resonant Compensation Control for Terminal Capacitance Reduction in Resonant Switched-Capacitor Converters," COMPEL 2021.



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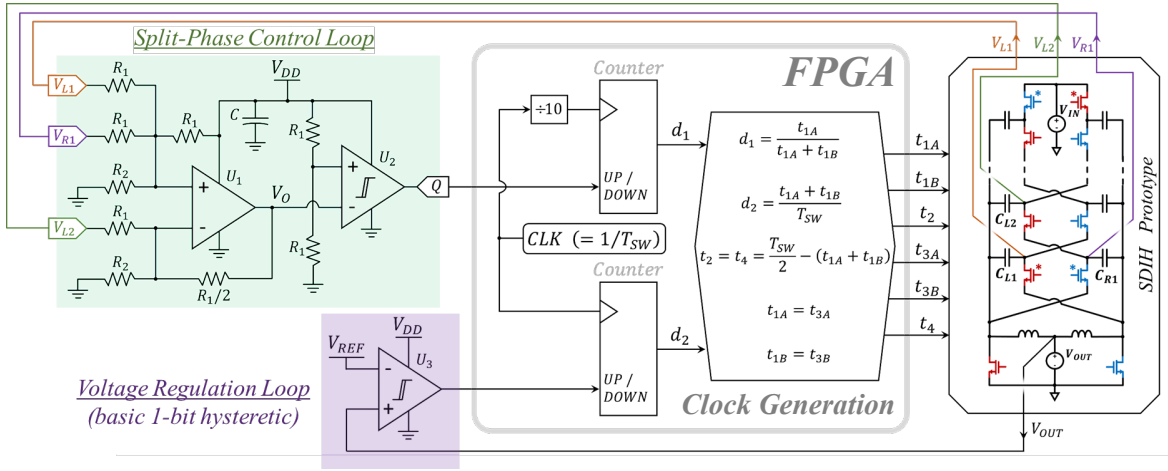
Closed-Loop Split-Phase Control Applied to a Regulating Point-of-Load (PoL) Dickson-Type Converter

Berkeley Power and Energy Center

Motivation and Application

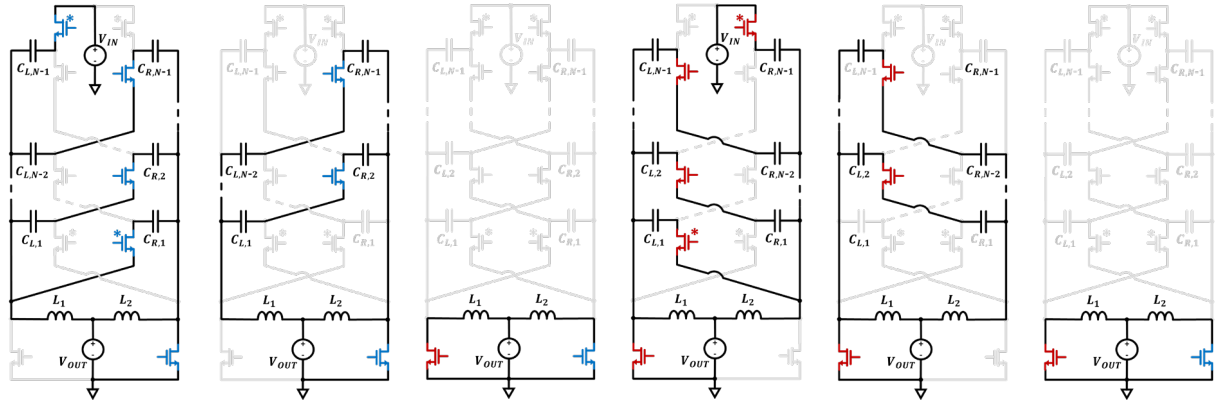
Hybrid Switched Capacitor (HSC) power converter topologies are being adopted in 48V to point-of-load (PoL) applications. Within the HSC converter class, Dickson-type converters [1] achieve the lowest Volt-Amp switch stress, indicative of a smaller semiconductor footprint for equivalent performance. However, some of these topologies require a non-conventional clocking scheme – recently coined as "split-phase switching" [2] – to ensure high efficiency is preserved. Executed in parallel with complimentary work in [3], this work presents a closed-loop split-phase control appropriate for regulating PoL converters [4]; over-coming a key obstacle to the deployment of a new and highly competitive class of hybridized power converter topologies.

Closed-loop Split-phase Control Demonstrated in Hardware



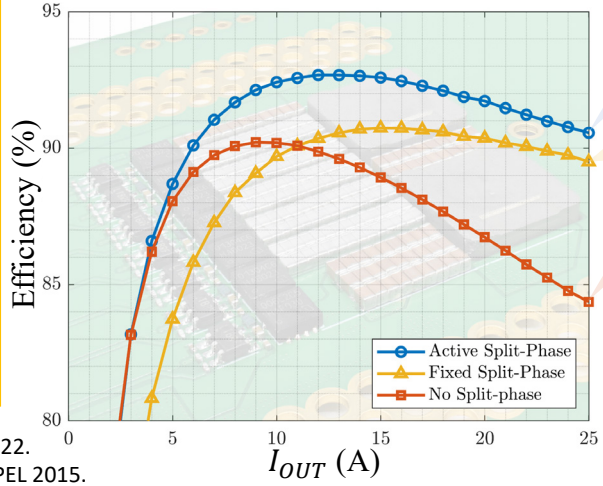
An added *Split-Phase Control Loop* detects "hard-charging" events and informs appropriate phase timing adjustments within a conventional FPGA-based clock generator.

Example: Phase Progression of the SDIH (Dickson-Type) Converter[4]



The duration of all phases are fully constrained as a function of V_{IN}, V_{OUT}, I_{IN}, f_{SW}, & component values. The practical inclusion of loss and component derating/mismatch necessitates continuous and dynamic phase duration adjustments.

Experimental Verification

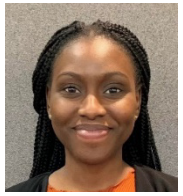


Closed-Loop Control

Theoretical Timings

Without Split-Phase Control

Operating Point	
V_{IN}	48V
V_{OUT}	3.3V
f_{SW}	300 kHz



[1] N. Ellis, R. Amirtharajah, "Large Signal Analysis on Variations of the Hybridized Dickson Switched-Capacitor Converter," TPEL 2022.
[2] Y. Lei, et. al., "Split-Phase Control: Achieving Complete Soft-Charging Operation of a Dickson Switched-Capacitor Converter," TPEL 2015.
[3] R. Abramson, et. al., "An Active Split-Phase Control Technique for Hybrid Switched-Capacitor Converters Using Capacitor Voltage Discontinuity Detection," COMPEL 2023.
[4] N. Ellis, et. al., "Closed-Loop Split-Phase Control Applied to the Symmetric Dual Inductor Hybrid (SDIH) Converter," COMPEL 2023.

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Active Soft-Charging Control for Hybrid and Resonant Switched-Capacitor Converters

Berkeley Power and Energy Center

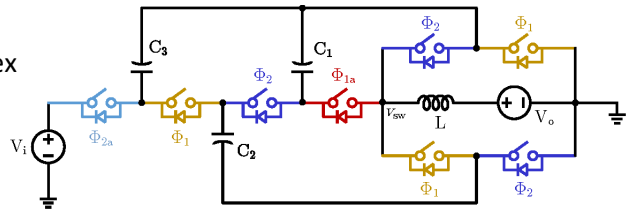
Motivation and Application

Dickson-derived converters are increasingly used for both **fixed-ratio** and **direct-to-PoL** applications in the datacenter and transportation space. They can achieve **very low switch stress** (i.e. Volt·Amp product), which means that lower-voltage (and therefore less lossy) switches can be used compared to other topologies for a given output power.

Split-Phase Control

Certain Dickson topologies require more complex **split-phase control schemes** [1] in order to achieve full soft-charging of all fly capacitors. Split-phase control timings can be complex to calculate and vary depending on **component tolerance, circuit non-idealities, and operating condition,** necessitating **active control** [2], [3].

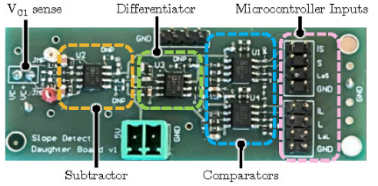
4:1 resonant Dickson converter

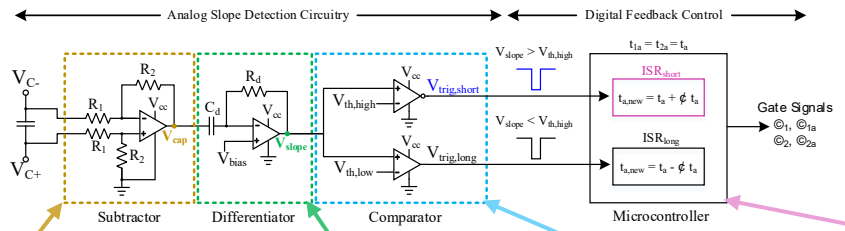


The conventional two-phase operation is split into phases {1a, 1b} and {2a,2b}

Analog Sensing Circuitry

Control Daughterboard





Differential capacitor voltage sensed and signal-conditioned

Slope detect circuit triggers on large step discontinuities

Polarity of step discontinuity shows whether split-phase timing is too short or too long

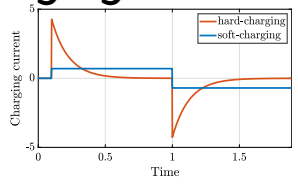
Interrupt service routine (ISR) increases or decreases split-phase timing accordingly

- The analog circuitry is flexible in implementation, and stages can be combined into single package op-amps or off-loaded into internal microcontroller comparator units to increase density.

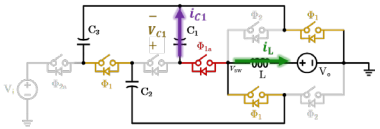
Capacitor Losses: Hard-Charging vs. Soft-Charging

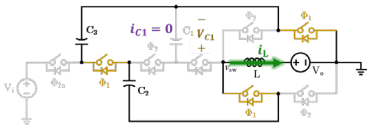
Hard-charging: large charge redistribution loss, spiky currents.

Soft charging: no charge redistribution loss, smooth / resonant currents.



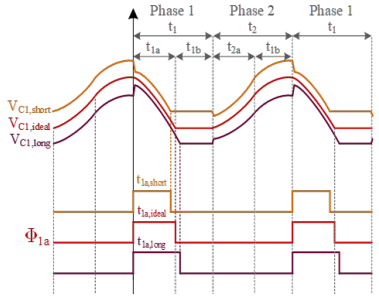
Phase 1 Split-Phase Operation





If the {1a,1b} and {2a,2b} transitions occur at the wrong time, hard-charging occurs, resulting in **current spikes** and **discontinuous capacitor voltages.**

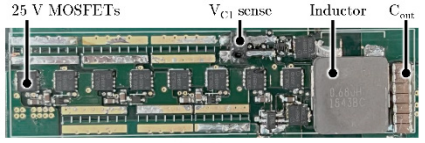
These voltage steps can be sensed, allowing the controller to auto-tune split-phase times to achieve soft-charging operation.



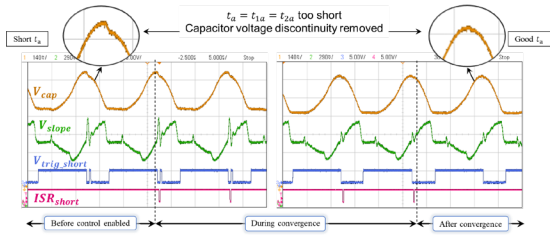
Experimental Verification

- An 8-to-1 resonant Dickson converter was used for validation.
- The control scheme was able to converge on soft-charging split-phase timing when 1) initialized in a hard charging-condition, and 2) when enabled during load step transients.

8:1 Dickson Converter

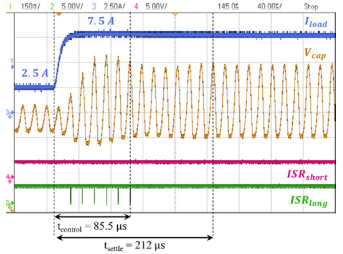


Steady-State Convergence



Smooth capacitor voltages signify soft-charging operation

Load Step Transient



Operating Conditions

Parameter	Value
V_{in}	48 V
V_{out}	6 V
$I_{out,max}$	10 A

References:

[1] Y. Lei et al., "**Split-Phase Control: Achieving Complete Soft-Charging Operation of a Dickson Switched-Capacitor Converter**", *IEEE Trans. on Power Electronics*, vol. 31, no. 1, pp. 770-782, 2015. [2] R. A. Abramson et al., "**An Active Split-Phase Control Technique for Hybrid Switched-Capacitor Converters Using Capacitor Voltage Discontinuity Detection**," *2023 IEEE 24th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Ann Arbor, MI, USA, 2023. [3] N. M. Ellis, H. Sambo and C. N. Robert Pilawa-Podgurski, "**Closed-Loop Split-Phase Control Applied to the Symmetric Dual Inductor Hybrid (SDIH) Converter**," *2023 IEEE 24th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Ann Arbor, MI, USA, 2023.

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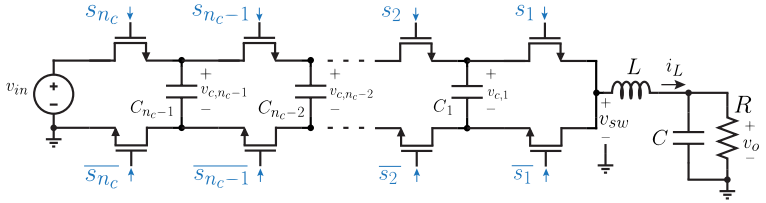
Closed-Loop Balancing Control and Capacitor Voltage Estimation for the Flying Capacitor Multilevel Converter

Berkeley Power and Energy Center

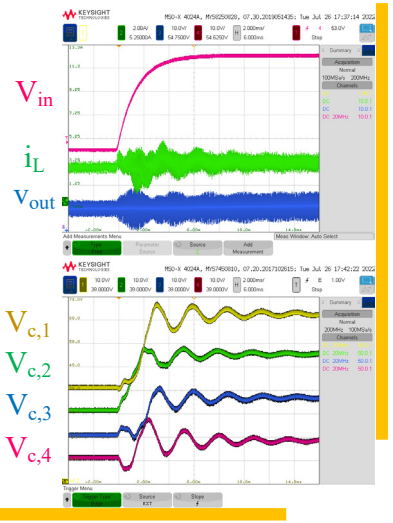
Balancing Control Motivation

Open-loop balancing of capacitor voltages is unreliable

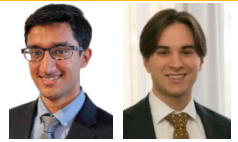
- Capacitor voltages during large-signal transients exhibit underdamped dynamics
- Peak switch stress may be greater than $\frac{V_{in}}{N-1}$ and can cause switch overvoltage in high-performance designs using low-voltage switches



Natural Balancing



Capacitor Voltage Estimation

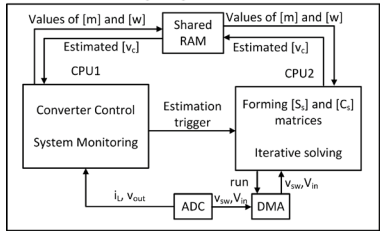


- Active balancing requires measurement of capacitor voltages
- Measuring each capacitor voltage with its own differential sensor is expensive
- Can instead measure switched-node voltage with single-ended sensor and calculate capacitor voltages
- Solve system of equations iteratively with reduced computation burden
- Demonstrated on industry-standard Texas Instruments C2000 DSP

$$\begin{bmatrix} v_{sw}^{I} \\ v_{sw}^{II} \\ v_{sw}^{III} \\ v_{sw}^{IV} \\ v_{sw}^{V} \\ v_{sw}^{VI} \end{bmatrix} = \begin{bmatrix} s_1^{I} & 0 & 0 & 0 & 0 & 0 \\ 0 & s_1^{II} & 0 & 0 & 0 & 0 \\ 0 & 0 & s_1^{III} & 0 & 0 & 0 \\ 0 & 0 & 0 & s_1^{IV} & 0 & 0 \\ 0 & 0 & 0 & 0 & s_1^{V} & 0 \\ 0 & 0 & 0 & 0 & 0 & s_1^{VI} \end{bmatrix} \begin{bmatrix} V_{in}^{I} \\ V_{in}^{II} \\ V_{in}^{III} \\ V_{in}^{IV} \\ V_{in}^{V} \\ V_{in}^{VI} \end{bmatrix} + \begin{bmatrix} s_2^{I} - s_1^{I} & s_3^{I} - s_2^{I} \\ s_2^{II} - s_1^{II} & s_3^{II} - s_2^{II} \\ s_2^{III} - s_1^{III} & s_3^{III} - s_2^{III} \\ s_2^{IV} - s_1^{IV} & s_3^{IV} - s_2^{IV} \\ s_2^{V} - s_1^{V} & s_3^{V} - s_2^{V} \\ s_2^{VI} - s_1^{VI} & s_3^{VI} - s_2^{VI} \end{bmatrix} \begin{bmatrix} v_{c1} \\ v_{c2} \end{bmatrix}$$

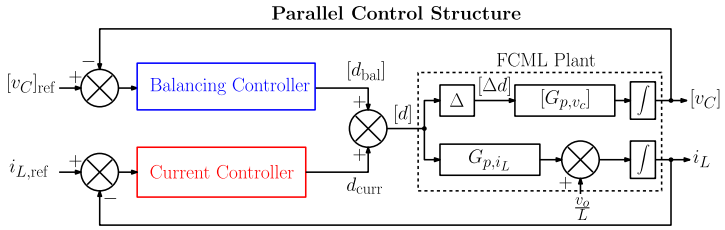
First cell's switch states — Capacitor connection matrix

Digital Signal Processor



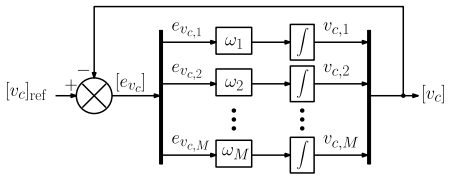
Closed-Loop Control

Parallel Control Structure

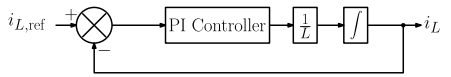


Equivalent Controllers after Decoupling and Feedback Linearization

Decoupled Balancing Control Loops



Decoupled Current Control Loop

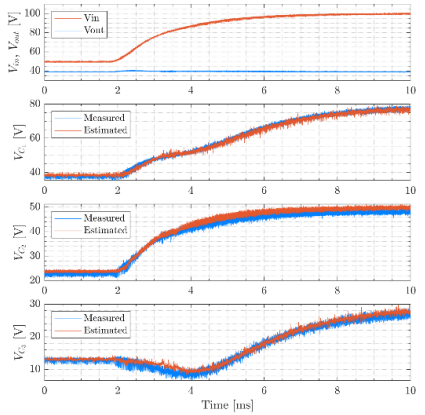


- Model average behavior of FCML converter to obtain "plant" for control
- Structure of plant informs controller design: duty ratios can be controlled differentially to steer capacitor voltages
- Balancing controller runs in parallel with controller(s) regulating load voltage
- Closed-loop system is decoupled – controllers operate without mutual interaction

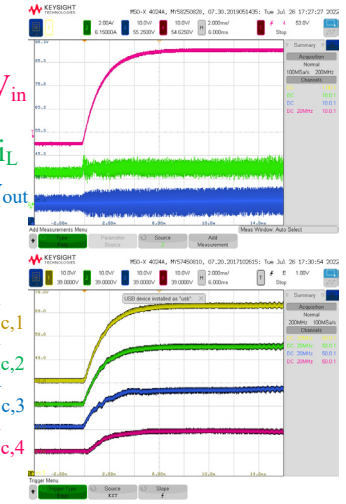
Experimental Verification

- Active balancing ensures capacitor voltages track nominal values during supply transients
- Single-sensor estimation of capacitor voltages is reliable and low-cost

Estimation



Active Balancing



References:
[1] R. K. Iyer, et al., "A High-Bandwidth Parallel Active Balancing Controller for Current-Controlled Flying Capacitor Multilevel Converters," 2023 IEEE Applied Power Electronics Conference and Exposition (APEC).
[2] I. Z. Petric, et al., "A Real-Time Estimator for Capacitor Voltages in the Flying Capacitor Multilevel Converter," 2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL).

Rahul Iyer (rkiyer@berkeley.edu), Ivan Petric (ivan.petric@phd.unipd.it)

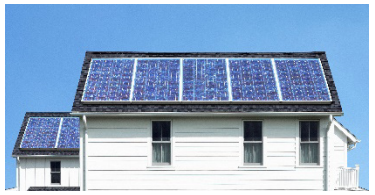
A Hybrid Switched-Capacitor Solar Microinverter Utilizing a Fixed-ratio Resonant DC-DC Stage and Flying Capacitor Multi-level DC-AC Stage

Berkeley Power and Energy Center

Motivation and Application

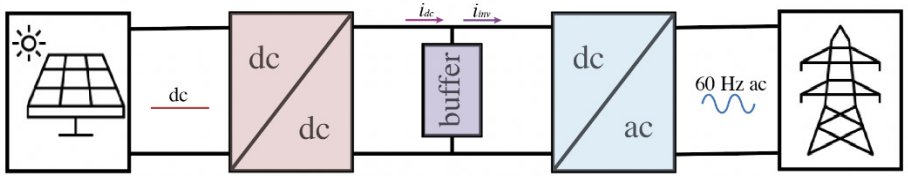
Hybrid Switched-Capacitor Converters

- The Cascaded Series-Parallel converter (CaSP) has been used as a power-dense dc-dc step-down solution in the 48V application space but is being adapted use as a boost stage [1].
- The flying capacitor multilevel converter (FCML) can be used to step down the



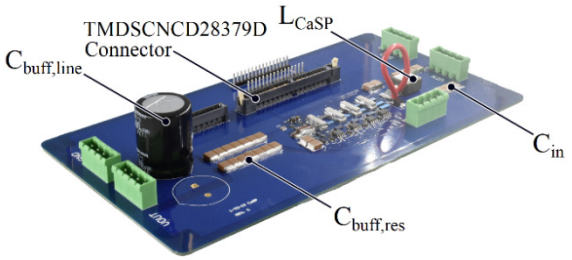
Rooftop solar requires **efficient** and **power dense** solutions to convert power for use in homes and at the grid.

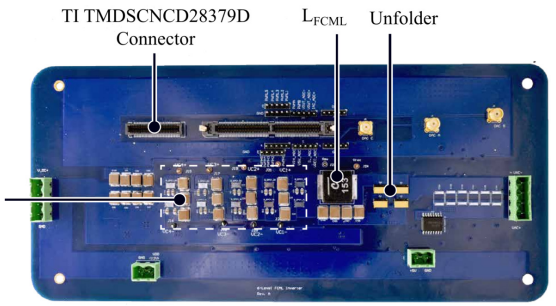
Example inverter: Enphase IQ8



Full microinverter concept.

Hardware





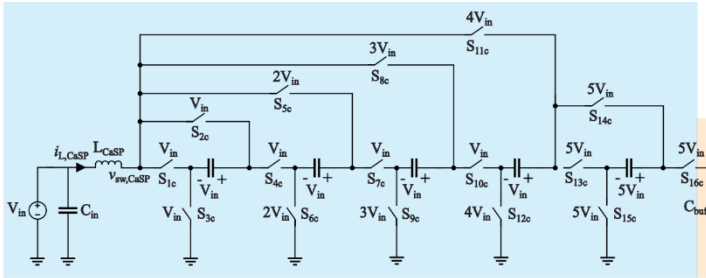
CaSP System Specifications

- 35-40V input
- 350-400V, 500W output

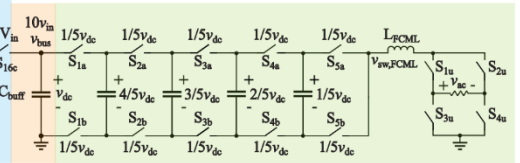
FCML System Specifications

- 350-400V input, 500W+
- Sensing for control included on this board.
- 2nd revision coming soon

System Architecture

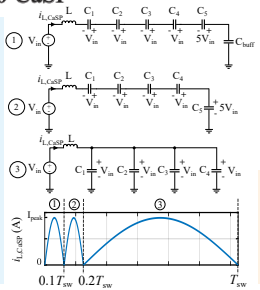


1-to-10 CaSP

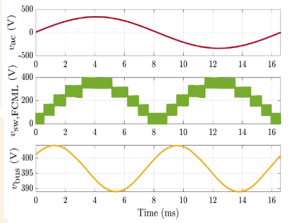


Buffer 6-Level FCML + Unfolder

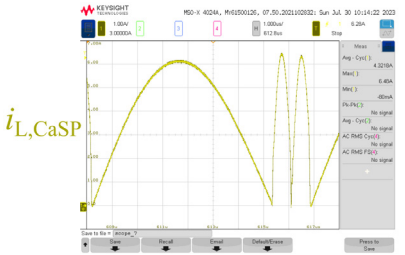
- Three sub-intervals of one switching cycle, each with a unique resonant LC tank impedance [2].
- Achieves ZCS, partial ZVS.
- Can be used as stand-alone startup circuitry.

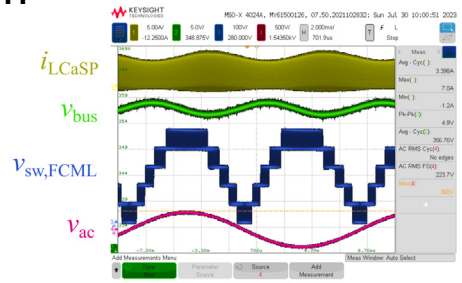


- 400V to 240Vac. Voltage at output of inductor is rectified sine wave that is unfolded by H-bridge.
- HV buffer allows for reduction of capacitance due to smaller current ripple



Experimental Validation





System waveforms with 240 V_{ac} output

Peak efficiency with 255 Vac output at light load: **93.5%**

- System able to produce 240 Vac output at light load
- CaSP achieves ZCS during full system operation at 240 Vac output

References:
[1] R. A. Abramson, Z. Ye, T. Ge and R. C. N. Pilawa-Podgurski, "A High Performance 48-to-6 V Multi-Resonant Cascaded Series-Parallel (CaSP) Switched-Capacitor Converter," 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), Phoenix, AZ, USA, 2021
[2] K. Fernandez and R. C. N. Pilawa-Podgurski, "A 1-to-10 Fixed-Ratio Step-up Multi-Resonant Cascaded Series-Parallel (CaSP) Switched-Capacitor Converter with Zero-Current Switching," *2023 11th International Conference on Power Electronics and ECCE Asia (ICPE 2023 - ECCE Asia)*, 2023

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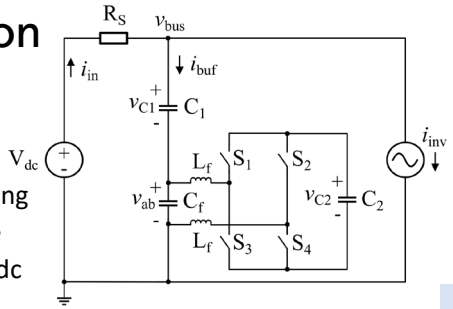
A Charge Injection Loss Compensation Method for a Series-Stacked Buffer to Reduce Current and Voltage Ripple in Single-Phase Systems

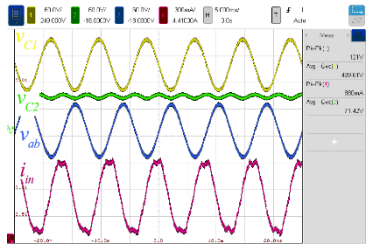
Berkeley Power and Energy Center

Motivation and Application

The Series-stacked buffer (SSB) is an active buffer topology that achieves high energy utilization and greatly decreases the power conversion system volume without comprising efficiency [2]. However, there can be a large amount of residual ac current ripple on the dc bus due to SSB's control methodology that injects real power through the reactive buffer branch. This control is required to charge the C_2 capacitor in the SSB that acts as a dc source for a full-bridge converter. Specifically, this ripple gets is worse in applications with low source impedance, such as battery systems.

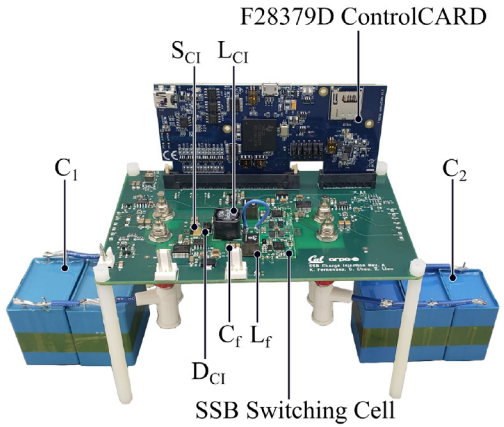


SSB circuit that handles reactive buffering. Real power is injected to charge C_2.



The real power injection causes large ac current ripple along the dc-link i_{in} (24% ac current ripple shown at 1.5 kW at 400 V_{dc}).

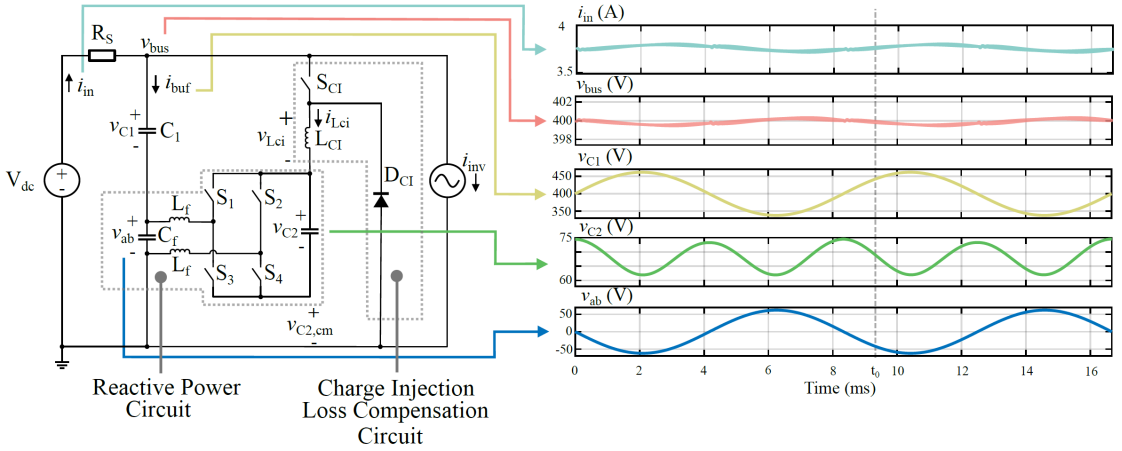
Hardware



Component	Part No.	Parameters
$S_1 - S_4$	EPC2033	150 V, 6 mΩ
S_{CI}	GaN Systems GS66506T	600 V, 2 A
D_{CI}	ON Semiconductor MURS160T3G	650 V, 67 mΩ
L_{CI}	Coilcraft MSS1210-104	100 µH
C_1	TDK B32524Q1686K000	100 V, 68 µF x 3
C_2	TDK B32776G4406K000	450 V, 40 µF x 2

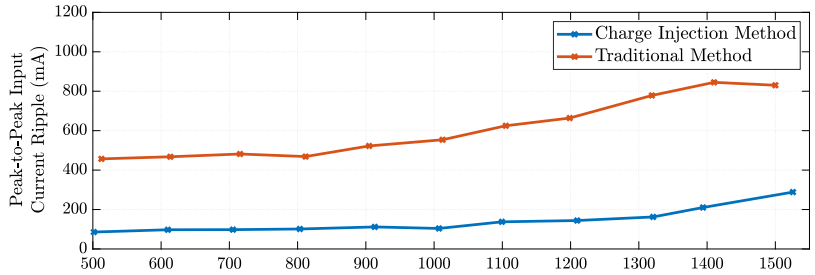
Proof of concept hardware. GaN devices are used for all switches. The volume of this design can be further reduced by using the optimization methodology shown in [3].

Proposed "Charge Injection" Method



The Charge Injection method has a separate branch that handles real power delivery while the rest of the SSB handles the reactive power buffering. As a result, the dc-link current ripple is greatly reduced.

Experimental Verification



The peak-to-peak ac current ripple is reduced:

- By maximum of **5.3x**
- And average of **4.3x**
- **3x** at peak load

Charge Injection method achieves an average **efficiency of 99.4%** across all loads.

References:
[1] K. Fernandez, N. Brooks, T. Ge, Z. Liao, R. C. N. Pilawa-Podgurski, "A Charge Injection Loss Compensation Method for a Series-Stacked Buffer to Reduce Current and Voltage Ripple in Single-Phase Systems" in 2022 Applied Power Electronics Conference (APEC), 2022.
[2] Z. Liao, et al. "A High Power Density Power Factor Correction Converter with a Multilevel Boost Front-End and a Series-Stacked Energy Decoupling Buffer," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), 2018, pp. 7229-7235,
[3] Z. Liao, et al. "Multi-objective optimization of series-stacked energy decoupling buffers in single-phase converters," in 2018 IEEE19th Workshop on Control and Modeling for Power Electronics (COMPEL), July 2018, pp. 1–7.

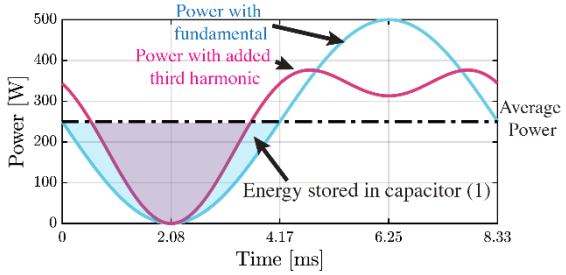
Student Name: Kelly Fernandez, kefernandez@berkeley.edu

Utilizing Harmonic Injection to Reduce Energy Storage in a Single-Phase Active Energy Buffer

Berkeley Power and Energy Center

Motivation

- Single-phase power converters rated for high power applications require reactive buffering on the dc bus to maintain a constant and clean dc power input or output. Often this is a bulky electrolytic capacitor.
- [1] found that buffer storage requirements for a passive buffer could be reduced 56% for the addition of allowable 3rd and 5th harmonics
- We apply this harmonic injection method for energy storage reduction in the capacitors of the series-stacked buffer (SSB), which is a power-dense alternative to the conventional capacitor solution.



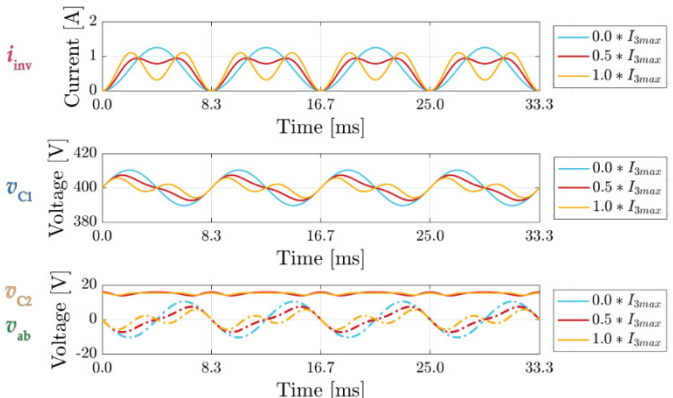
Energy storage in buffer during a twice-line frequency cycle.

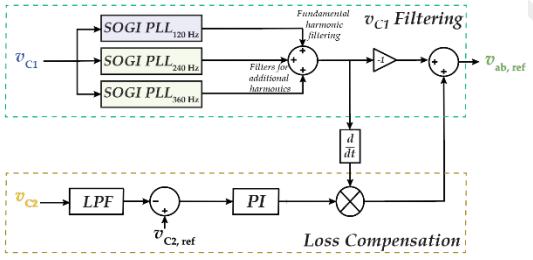
$$W_{store} = \int_0^{\frac{T_{2l}}{2}} P_{buff}(t)\,\mathrm{d}t$$

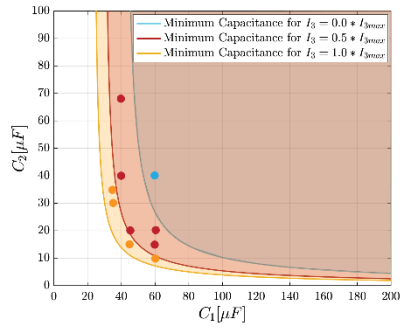
$$W_{store} = \frac{1}{2}CV_{max}^2 - \frac{1}{2}CV_{min}^2$$

Challenges and Control

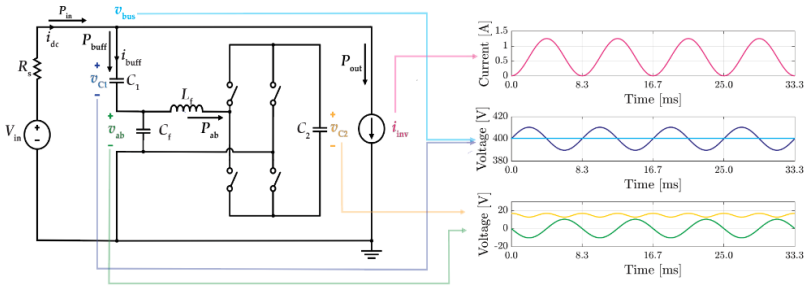
- Determining the expected voltage ripple on each of the capacitors is nontrivial.
- Figure out how to control an active buffer when additional harmonics are added to the system.

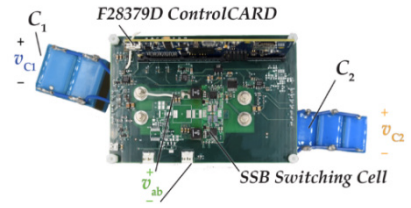






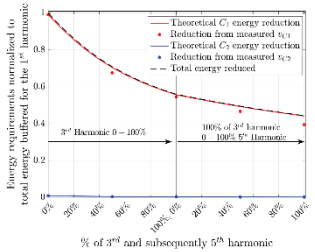
Circuit Topology and Hardware

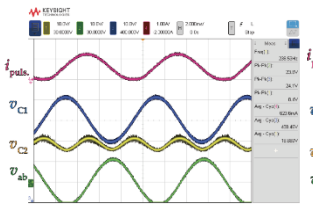




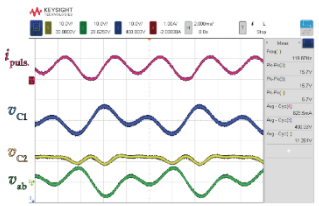
The SSB is an active buffer that combines a primary energy buffer capacitor with an H-bridge. This permits a larger voltage ripple across the main energy storage capacitor maximizing the amount of energy buffered, and subsequently the energy utilization ratio [2].

Experimental Verification

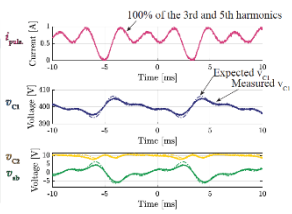




No harmonic.



Third harmonic.



Third and fifth harmonics.

55% reduction in required energy storage split between two capacitors. In an example case, C_1 can be reduced from $60\mu F$ to $34\mu F$, and C_2 from $27\mu F$ to $20\mu F$ for same dc-bus voltage ripple [3].

References:
[1] A. J. Hanson, A. F. Martin, and D. J. Perreault, "Energy and Size Reduction of Grid-Interfaced Energy Buffers Through Line Waveform Control," *IEEE Transactions on Power Electronics*, Nov. 2019
[2] N. C. Brooks, S. Qin, and R. C. N. Pilawa-Podgurski, "Design of an active power pulsation buffer using an equivalent series-resonant impedance model," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics*, Jul. 2017
[3] F. Giardine, N. C. Brooks, K. Fernandez and R. C. N. Pilawa-Podgurski, "Utilizing Harmonic Injection to Reduce Energy Storage and Required Capacitance in an Active Series-Stacked Energy Buffer for Single-Phase Systems," *2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics*, 2022

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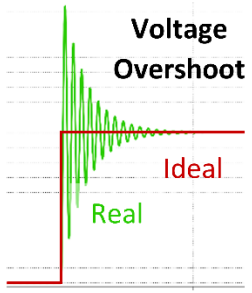
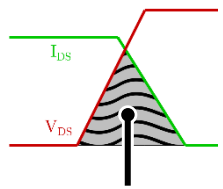
Advanced Switching Cell Design Techniques

Berkeley Power and Energy Center

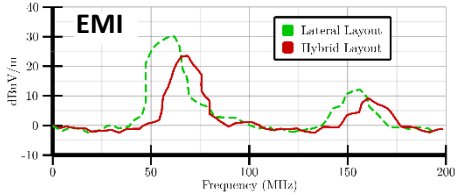
Motivation and Application

Power converters operate by switching between different circuit states. Ideally, the switching transitions would be instantaneous and lossless. In reality, parasitic effects cause switching losses, voltage overshoot, and electromagnetic interference. Advanced design techniques are presented here, which mitigate these effects and enable unprecedented performance.





Switching Loss



Interleaved Commutation Loop Layout [2]

Commutation loop inductance is critical to switching performance. Advanced layout techniques can be utilized to reduce this inductance.

Interleaved hybrid decoupling capacitor loops with electrically thin vertical bulk capacitor loop

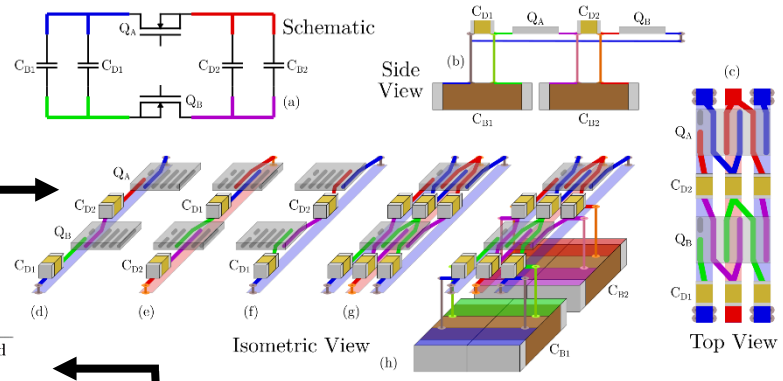
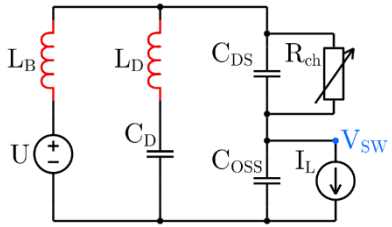


Table 1: Commutation Loop Comparison

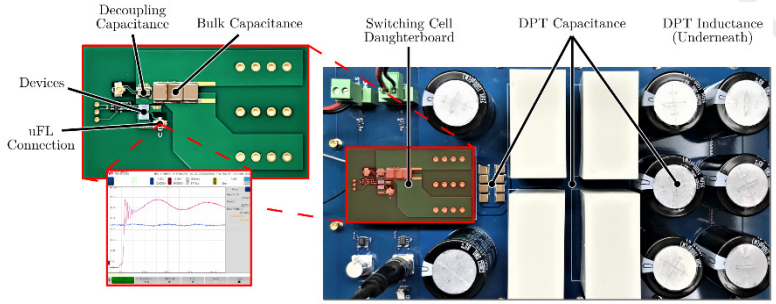
Switching Cell Design	Electrically Thin	Hybrid & E-thin	Hybrid Reference	Proposed Design
Simulated Inductance	1.15 nH	450 pH	521 pH	443 pH
Measured Inductance	2.85 nH	940 pH	—	1.14 nH
Board Area	370 mm²	330 mm²	420 mm²	420 mm²

- Proposed design achieves nearly 3x better performance than best approach without decoupling capacitors
- 20% better than state of the art

Optimal Decoupling Capacitor Sizing [1]

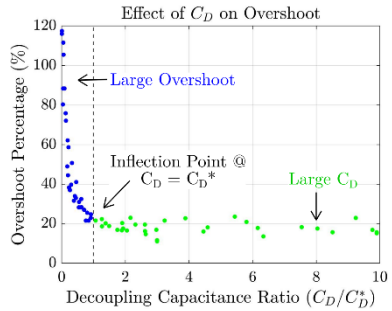


Simplified Switching Circuit Model



Double Pulse Test Hardware Setup

Experimental Data



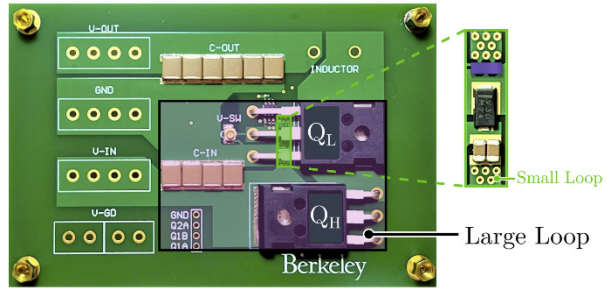
Determined optimal decoupling capacitor size given load current and output capacitance of the device:

$$C_D^* = 10 * \max\{C_{OSS}, 2L_B I_{ML}^2 / U_{ML}^2\}$$

Decoupling Device [3]

For many applications, transistors with large through-hole packages are used, due to their high power handling capability. In this work, a small surface-mount gallium-nitride transistor is added to improve switching performance.

Buck converter hardware prototype



50% reduction in losses

References:
[1] L. Horowitz and R. C. N. Pilawa-Podgurski, "On Decoupling Capacitor Size in GaN-Based Power Converters," 2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL), Tel Aviv, Israel, 2022, pp. 1-5, doi: 10.1109/COMPEL53829.2022.9830000.
[2] L. Horowitz and R. C. N. Pilawa-Podgurski, "Modular Switching Cell Design for High-Performance Flying Capacitor Multilevel Converter," 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), Houston, TX, USA, 2022, pp. 342-347, doi: 10.1109/APEC43599.2022.9773604.
[3] L. Horowitz, N. M. Ellis and R. C. N. Pilawa-Podgurski, "Decoupling Device for Small Commutation Loop and Improved Switching Performance with Large Power Transistors," 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 2023, pp. 2620-2624, doi: 10.1109/APEC43580.2023.10131426.

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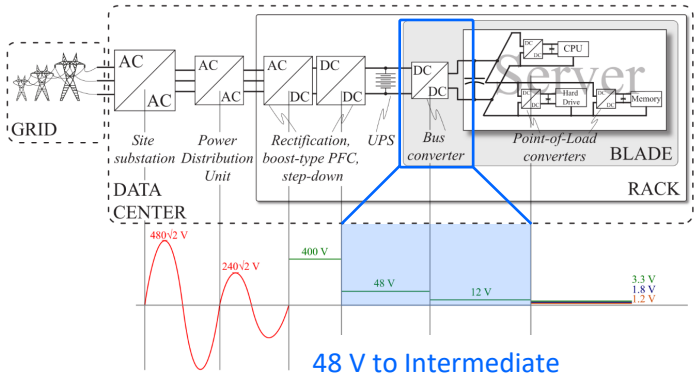
High-Performance 48-to-12 V Cascaded Multi-Resonant Switched-Capacitor Converter for Datacenters

Berkeley Power and Energy Center

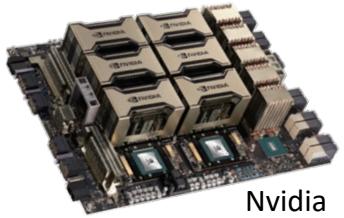
Motivation and Applications

48 V data center power delivery architecture



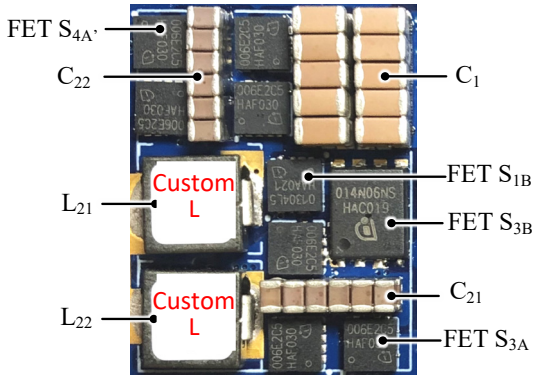
48 V to Intermediate Bus (IB) Converter

- The intermediate bus converter in 48 V data center application requires high efficiency and high power density
- Regulation and isolation are not required

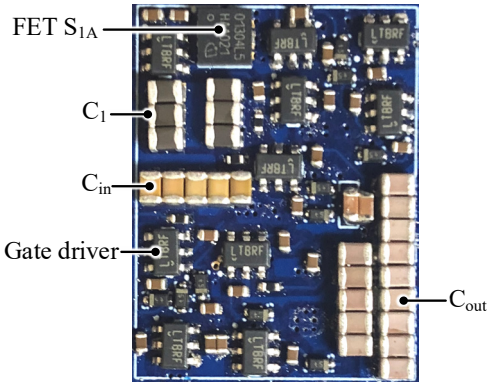


Nvidia

Hardware Demonstration



Top

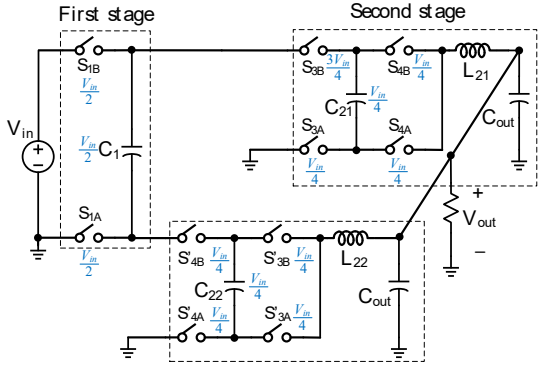


Bottom

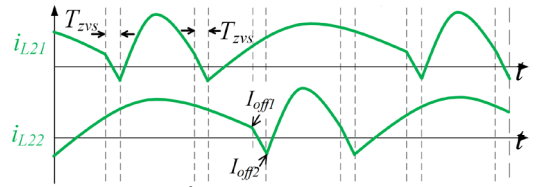
- Dimensions: 17.3 × 23 × 6.6 mm power density: **6000 W/in³** at 12 V output
- **80 A** continuous output and **130 A** - 2 ms transient output

Proposed Topology

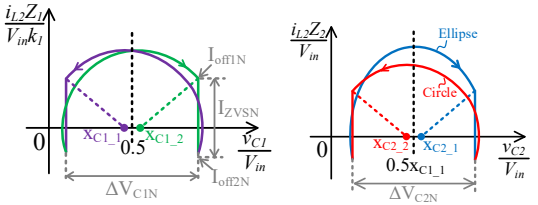
- Cascaded Multi-Resonant converter
- 1st stage uses only two switches to the save space of active components, and gate drive level shifters



- State-plane method is used to calculate multi-resonant inductor current

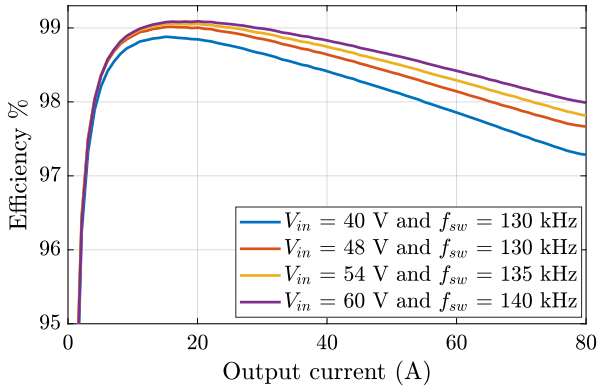


Inductor current

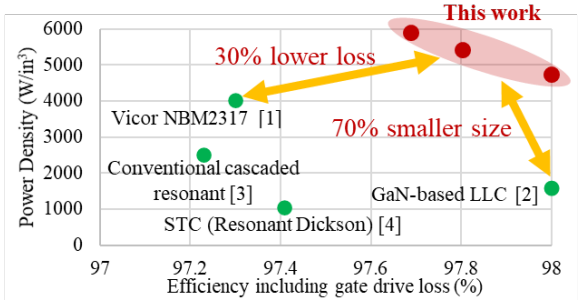


State trajectories of C_1L and C_2L

Experimental Results



Measured efficiencies including gate drive loss



Comparison with State-of-the-Art 48-to-12 V Solutions

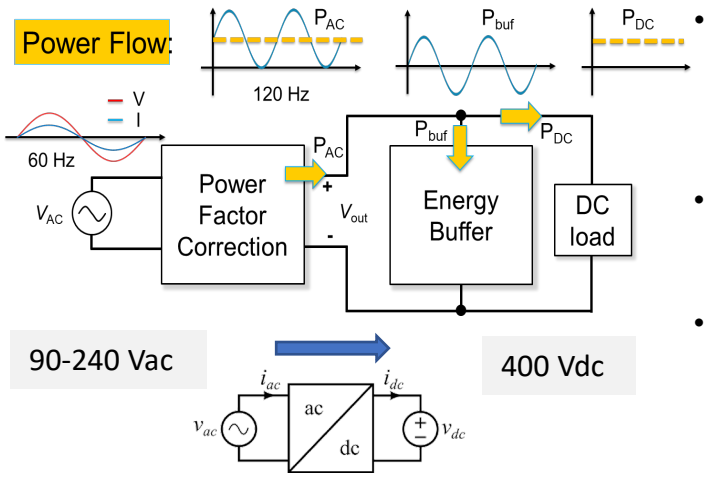
Reference: T. Ge, Z. Ye and R. C. N. Pilawa-Podgurski, "A 48-to-12 V Cascaded Multi-Resonant Switched Capacitor Converter with 4700 W/in3 Power Density and 98.9% Efficiency," 2021 IEEE ECCE.

Ting Ge Email: gting@berkeley.edu

High Performance Single-phase Ac-dc Conversion with Advanced Topology and Control

Berkeley Power and Energy Center

Motivation and Application



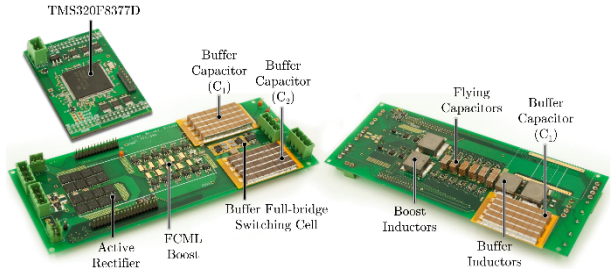
- 90-240 Vac to 400 Vdc is a critical conversion stage for applications such as data center power delivery, electric vehicle charging, etc.
- Ac-dc power factor correction

  Reduce boost inductor size
- Twice-line frequency power ripple buffering

  Reduce buffer capacitor size

Hardware Implementation

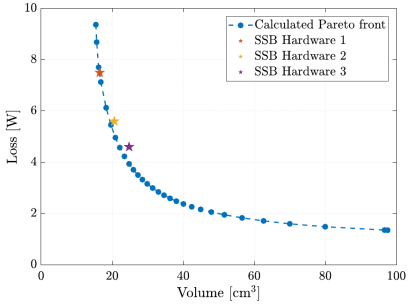
90-240 Vac to 400 Vdc, 1.5 kW PFC converter [1]



- Single DSP TMS320F28377D for the proposed system control
- GaN System and EPC GaN FETs used in FCML and SSB for high efficiency

Multi-objective optimization for SSB [2]

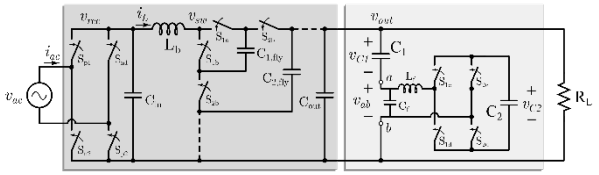
Loss-volume Pareto front of SSB generated with numerical optimization method



$$\min_{C_1, C_2, V_{C2,dc}} \quad \alpha \cdot \frac{f_{loss}}{F_{loss,\,max}} + (1-\alpha) \cdot \frac{f_{volume}}{F_{volume,\,max}}$$
$$s.t. \quad g_i \le 0 \quad \forall i = 1, .., 4.$$

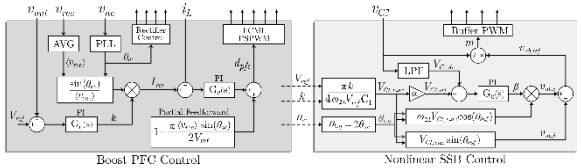
Challenges and Solutions

Topology



- The boost inductor size is reduced flying capacitor multilevel (FCML) topology
- An active buffer topology - series-stacked buffer (SSB) is implemented to reduce the buffer capacitor for twice-line frequency power ripple buffering

Control

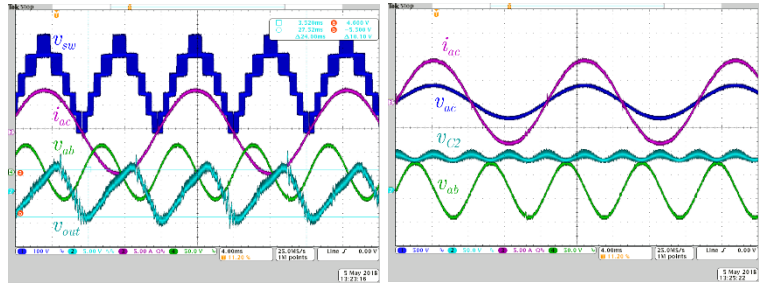


PFC+SSB Coupled Control:

- **PFC Multi-loop control**: high-bandwidth "inner" current & low-bandwidth "outer" voltage loop
- **PFC Partial feedforward** cancels the input voltage disturbances to input current caused by smaller boost inductor in FCML
- **Buffer control** obtains phase and amplitude information from PFC

Experimental Verification

Total box-volume power density:	**230 W/in³**
Peak efficiency:	98.9%
1.5 kW efficiency:	98.1%
THD:	< 5%
Power factor:	> 0.994



Experimental waveforms demonstrating power factor correction, multi-level switching, and SSB @ 1.5 kW, 240 Vac to 400 Vdc

References:
[1] Z. Liao. N. C. Brooks, and R. C. N. Pilawa-Podgurski, "A high power density power factor correction converter with a multilevel boost front-end and a series-stacked energy decoupling buffer," in 2018 IEEE Energy Conversion Congress and Exposition (ECCE), 2018
[2] Z. Liao, et al. "Multi-objective optimization of series-stacked energy decoupling buffers in single-phase converters," in 2018 IEEE19th Workshop on Control and Modeling for Power Electronics (COMPEL), July 2018, pp. 1–7.

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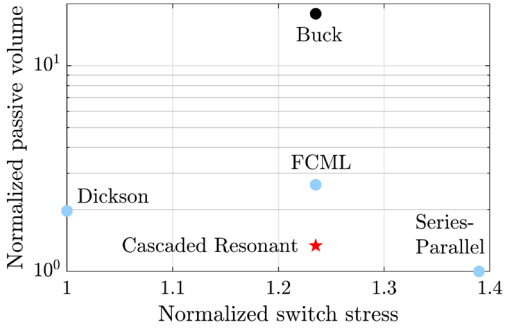
High Efficiency High Power Density Hybrid/Resonant Switched-Capacitor Converter

Berkeley Power and Energy Center

Theoretical Analysis



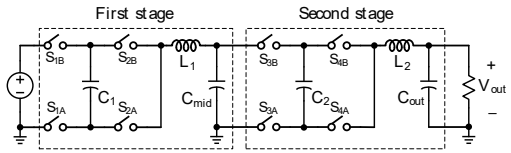
- Systematically analyze and calculate switch and passive utilization
- Compare and select the most suitable topology depending on application and power level
- Develop control technique to achieve soft-charging and soft-switching

Switch VA rating

$$\left(\sum_{switches} V_{ds} I_{ds}\right)$$

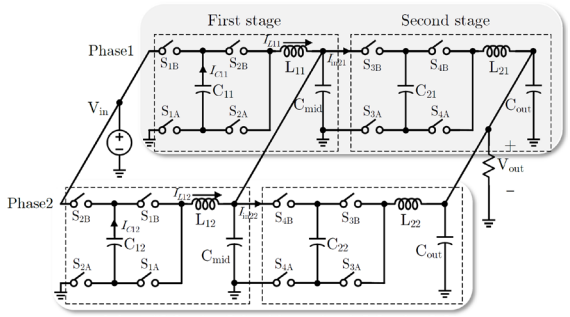
Total passives volume

$$\left(\frac{\frac{1}{2}\sum CV^2}{\rho_{E,C}} + \frac{\frac{1}{2}\sum LI^2}{\rho_{E,L}}\right)$$



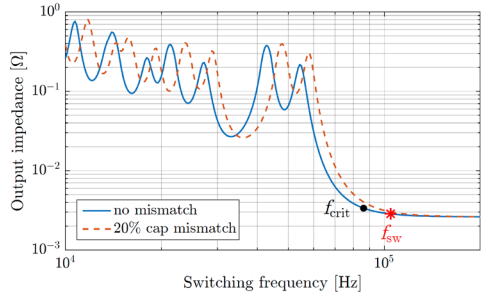
Cascaded Resonant Converter

Two-phase interleaved design



- Overcome the intermediate decoupling challenge of doubler topology

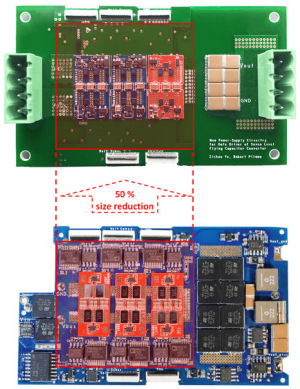
Zero voltage switching technique



- Operate the tank in the inductive region to achieve ZVS, while improving tolerance of component variations

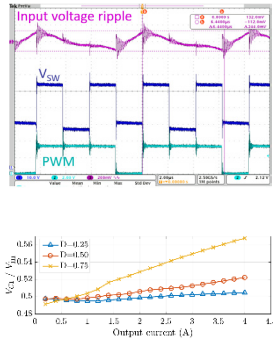
Practical Challenges and Solutions

Floating gate drive



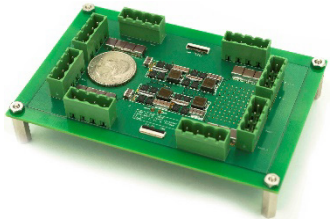
- Improved bootstrap and charge pump techniques to replace isolated dc/dc power supplies
- Achieving higher efficiency, lower cost and smaller footprint
- Working on system level circuit integration to further reduce size and cost

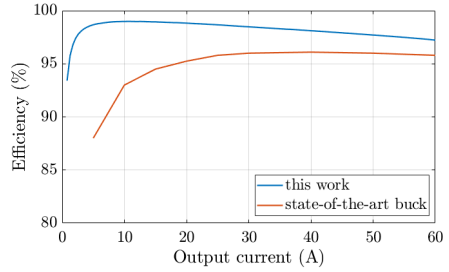
Capacitor voltage balancing



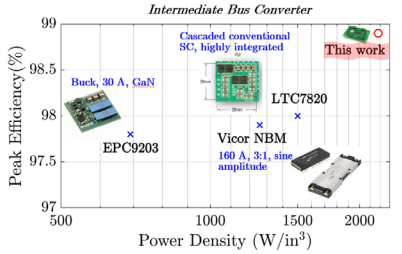
- Experimentally verified that source impedance and input capacitance can affect balancing drastically
- Even-level FCML converter has better natural balancing
- Gate drive voltage and signal mismatch can cause imbalance

Experimental Verification





Comparison with state-of-the-art



References:

[1] Z. Ye, Y. Lei, W. Liu, P. S. Shenoy and R. C. N. Pilawa-Podgurski, "Design and implementation of a low-cost and compact floating gate drive power circuit for GaN-based flying capacitor multi-level converters," *APEC 2017*

[2] Z. Ye, Y. Lei, Z. Liao and R. C. N. Pilawa-Podgurski, "Investigation of capacitor voltage balancing in practical implementations of flying capacitor multilevel converters", *COMPEL 2017*

[3] Z. Ye, Y. Lei and R. C. N. Pilawa-Podgurski, "A resonant switched capacitor based 4-to-1 bus converter achieving 2180 W/in3 power density and 98.9% peak efficiency," *APEC 2018*

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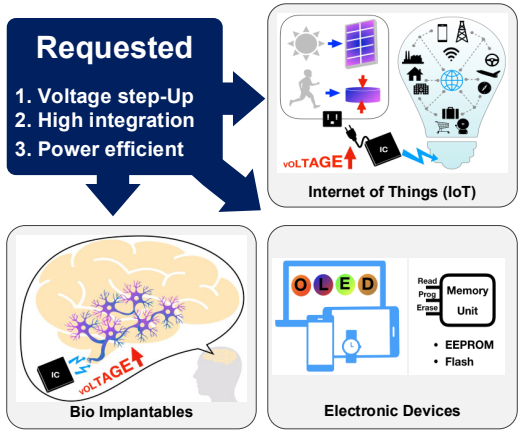
An 83mA 96.8% Peak Efficiency On-Chip 3-Level Boost Converter with Full-Range Auto-Capacitor-Calibrating Pulse Frequency Modulation (ACC-PFM)

Berkeley Power and Energy Center

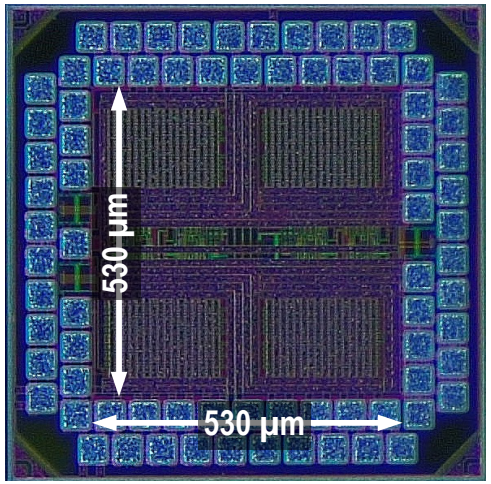
Motivation and Applications



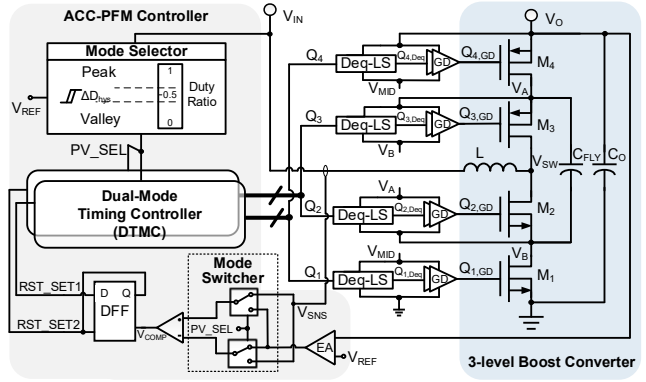
High voltages are demanded to

- Generate efficacious stimulations for bio-implantable devices
- Interface between low-voltage energy harvesters and batteries for wireless sensor network (WSN)
- Program memories for high operational speeds
- Drive LED strings efficiently

Chip Implementation

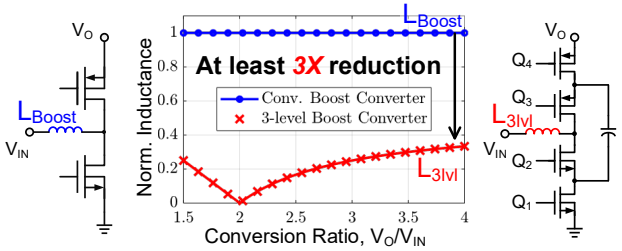


- TSMC 65nm CMOS process
- 2.5V devices for 5.0V operation



Challenges and Solutions

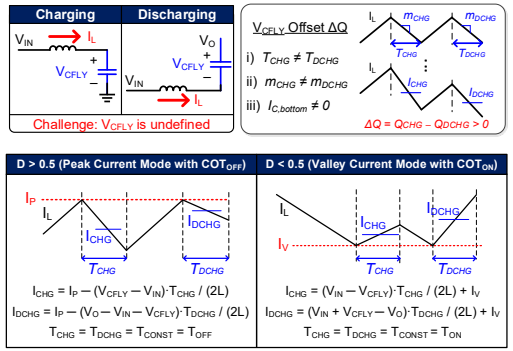
Topology: 3-level Boost Converter



Hybrid SC converters merge the advantages of the conventional switched capacitor (SC) and switched inductor converters (e.g. Boost converter)

- Achieve high power density
- Mitigate charge sharing loss in SC converter
- Retain the ability to employ low voltage

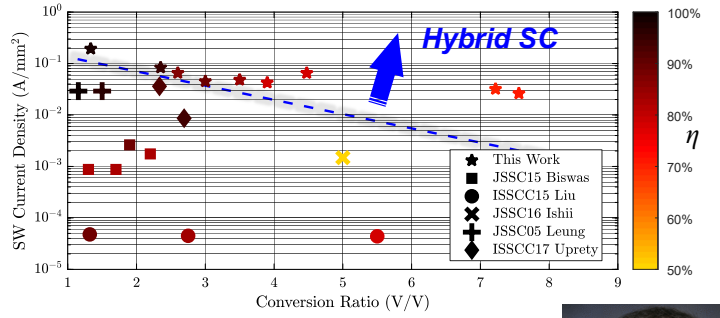
Control: ACC-PFM



- ACC-PFM is an integrated controller solution for both V_{OUT} regulation and capacitor balancing

Measurement Results

Peak Efficiency	96.8%
Input Voltage	0.3 – 3V
Output Voltage	2.4 – 5V
Peak Output Current	83 mA
Peak Switch Current Density	300 mA/ mm²
Switching Freq.	0.5M – 45MHz

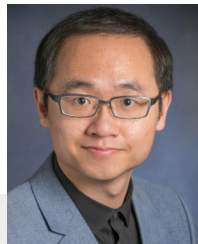


Excellent performance for wide-range voltage and load variation required in step-up applications, compared to prior arts.

References:

Wen-Chuen Liu, Pei Han Ng, Robert C.N. Pilawa-Podgurski, "An 83mA 96.8% Peak Efficiency 3-Level Boost Converter with Full-Range Auto-Capacitor-Calibrating Pulse Frequency Modulation", *IEEE Custom Integrated Circuits Conf.* ***(CICC)***, 2019.

Student: Wen-Chuen Liu Email: joseph.wcliu@berkeley.edu



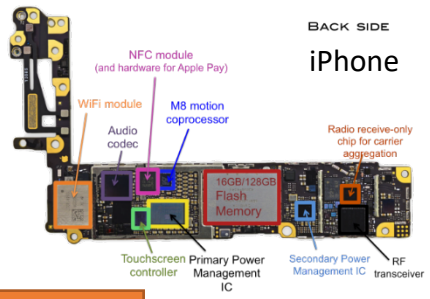
A 94.2%-peak-efficiency 1.53A direct-battery-hook-up hybrid Dickson switched-capacitor DC-DC converter with wide continuous conversion ratio in 65nm CMOS

Berkeley Power and Energy Center

Motivation and Application

Increased power density of advanced CMOS nodes in embedded applications requires the power converters to have:

- Higher efficiency to extend the battery life
- Low loss to ease the thermal management
- Higher power density to match the technology
- Maintain performance at large conversion ratios



Typical Battery voltage 3.2 V to 4.2 V

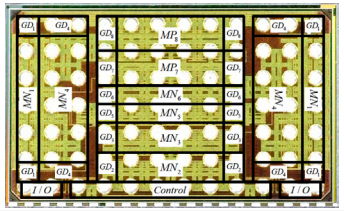
Typical Load voltage 300m V to 1 V

Typical Load current several mA to several A

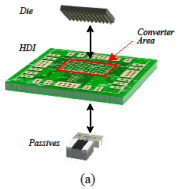
Increasing Gap

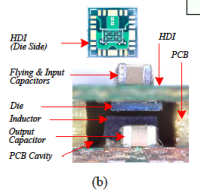
Hardware

- Implemented in CMOS 65nm bulk process
- Flip-Chip packaging for low parasitic
- Voltage borrowing gate drive to eliminate bootstrap capacitors and increase power density
- Active capacitor balancing and output regulation
- External flying capacitors and inductor
- High density interposer for uModule assembly

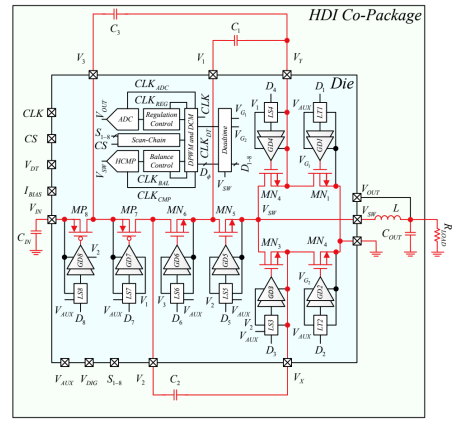


Die
4 mm2





uModule
Assembly



System Architecture

Challenges and Solutions

Utilized hybrid switched-capacitor (SC) converters.

Switched-Capacitor stage:

- Higher efficiency at large conversion ratios
- Lower rated devices for advance CMOS integration
- Poor regulation

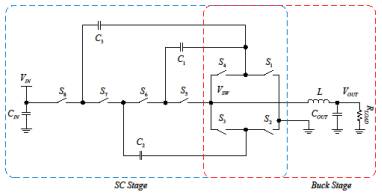
Magnetic Buck stage:

- Achieve tighter regulation
- Lower voltage swing for smaller magnetics

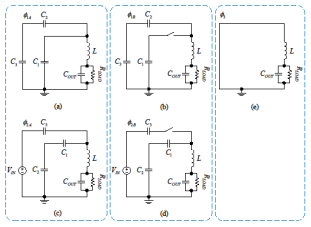
Need higher utilization of passive and active devices:

- Dickson SC has good switch utilization and poor capacitor utilization
- Soft-charging through split-phase control increases capacitor utilization, enhances efficiency and lower switching frequency
- Smaller passives for faster transient response and tighter control

4:1 Hybrid Dickson



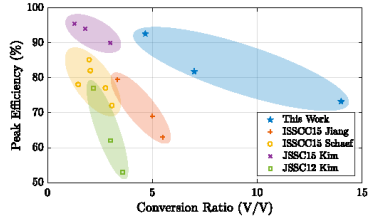
Split-Phase Control

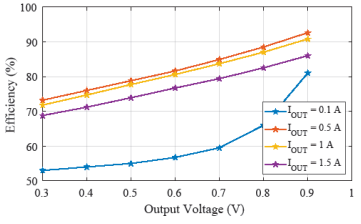


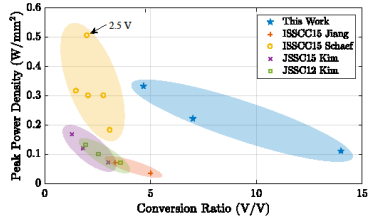
Experimental Verification

Maintained efficiency and power density:

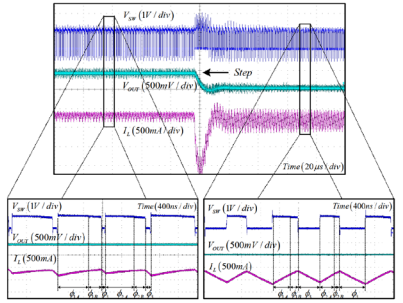
- Across large conversion ratios
- Across large load current range





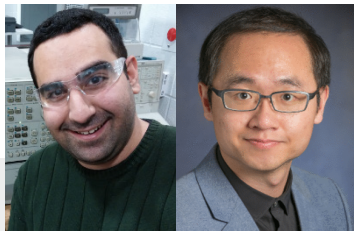


Output regulation and flying capacitor active balancing



Reference: W. Liu, P. Assem, Y. Lei, P. K. Hanumolu and R. Pilawa-Podgurski, "10.3 A 94.2%-peak-efficiency 1.53A direct-battery-hook-up hybrid Dickson switched-capacitor DC-DC converter with wide continuous conversion ratio in 65nm CMOS," *ISSCC 2017*.

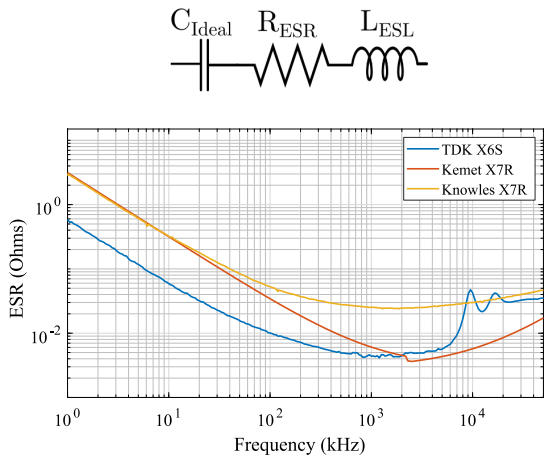
Pourya Assem: pourya_assem@Berkeley.edu
Wen-Chuen Liu: joseph.wcliu@Berkeley.edu



Characterization of Multi-layer Ceramic Capacitors under More Realistic Operating Conditions

Berkeley Power and Energy Center

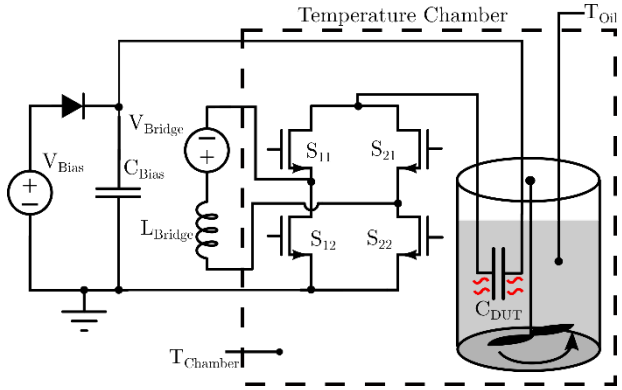
Motivation and Applications



- Multi-layer ceramic capacitors (MLCCs) are a key enabling technology for high density power converters.
- Real losses in MLCCs can be reduced to equivalent series resistance (ESR)
- Data sheets do not provide loss information for realistic operating conditions.

Hardware Implementation

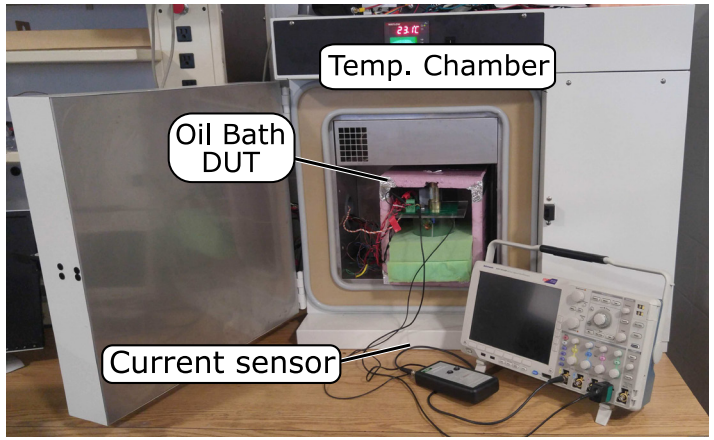
- ESR is dependent on frequency, DC bias, AC amplitude, temperature and harmonic content.
- A circuit was designed to be able to adjust frequency, current amplitude and DC bias of a high harmonic content waveform in order to test the effect on ESR.



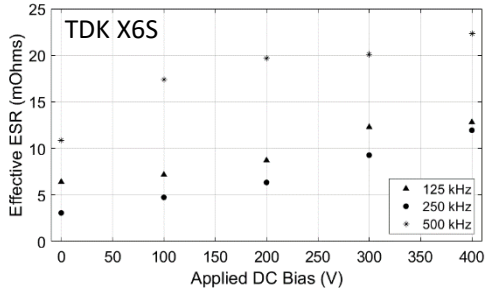
Challenges and Solutions

$$P_{diss} = \frac{1}{T_{final}} \left(k_{oil}\, \Delta temp + \int_0^{T_{final}} \frac{temp_{oil} - temp_{amb}}{R}\, dt \right)$$ [1]

- Measuring loss with electrical characterization is in accurate under desired operating conditions.
- A calorimetric method was implemented in order to accurately observe change in ESR.



Experimental Results



Capacitor Manufacturer	Capacitor De-rating (at 400 V)	ESR increase (at 400 V, 125 kHz)
TDK	80%	200%
Knowles	82%	243%
Kemet	72%	142%

- With increased DC bias, the ESR linearly increases, this has been shown with several dielectric types as well as manufacturers.

References:

[1] G. S. Dimitrakakis, E. C. Tatakis, and A. C. Nanakos, "A simple calorimetric setup for the accurate measurement of losses in power electronic converters," *EPE 2011*.

[2] S. Coday, C. B. Barth and R. C. N. Pilawa-Podgurski, "Characterization and Modeling of Ceramic Capacitor Losses under Large Signal Operating Conditions," *COMPEL 2018.*

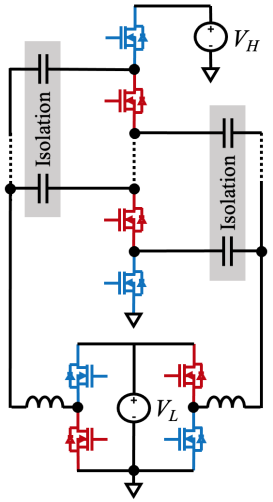
Student: Samantha Coday
Email: scoday@berkeley.edu

Hybrid Switched-Capacitor DC-DC Converters with Isolation

Berkeley Power and Energy Center

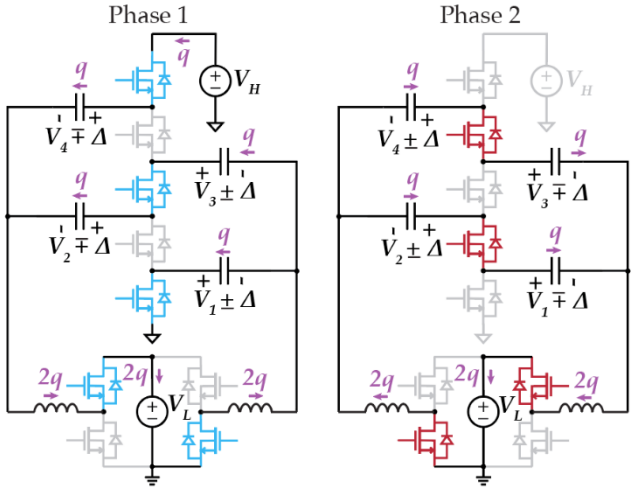
Motivation and Applications

- Hybrid switched-capacitor converters offer high power density but have been restricted to non-isolated applications
- Traditional isolation methods require bulky and heavy transformers
- Capacitive isolation presents a power-dense alternative to magnetic isolation
- Flying capacitors with high voltage rating act as isolation capacitors



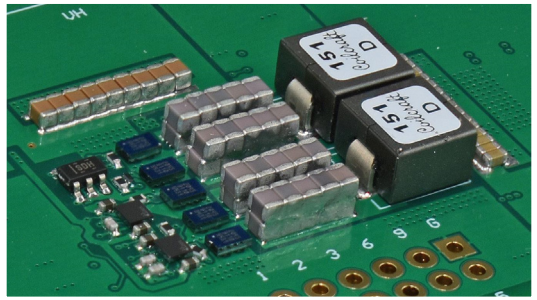
Theory of Operation

- Capacitively isolated hybrid switched-capacitor converter based on [1], [2]
- Complete soft-charging of capacitors eliminates loss from transient inrush currents
- 50% duty cycle and two-phase operation
- Switch voltage stress independent of load



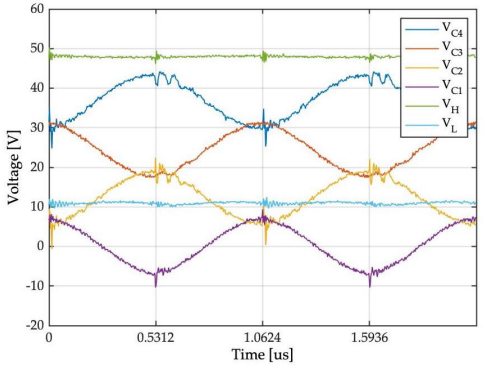
Challenges and Solutions

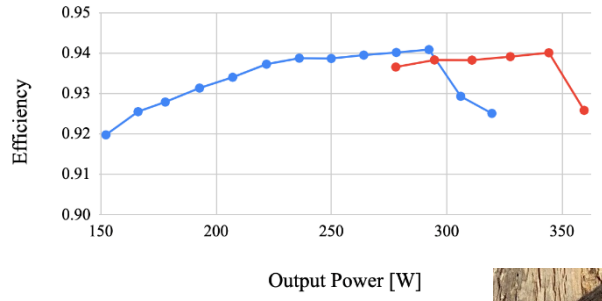
- ZVS theoretically possible, but not successful at higher input voltages
  - Ongoing issue; we'll spend more time investigating timing
- Light-load oscillations that damage converter at higher voltages
  - Current solution: avoid light load



Experimental Results

- 94.1% peak efficiency, 2,010 W/in^3 power density





[1] Y. Li, L. Gu, A. Hariya, Y. Ishizuka, J. Rivas-Davila, and S. Sanders,"A wide input range isolated stacked resonant switched-capacitor dc-dc converter for high conversion ratios," in *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2018, pp. 1–7.
[2] N. M. Ellis and R. Amirtharajah, "A resonant dual extended lc-tank dickson converter with 502021 *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 1282–1287.

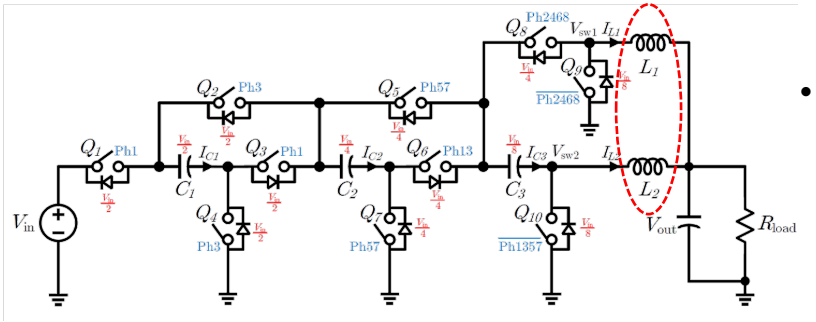
Student: Amanda Jackson Email: amandajackson@berkeley.edu

Core Size Scaling Law of Two-Phase Coupled Inductors – Demonstration in a 48-to-1.8 V MLB (Multi-Level-Binary)-PoL Converter

Berkeley Power and Energy Center

Motivation and Applications

Multi-Level Binary (MLB) hybrid switched-capacitor converter for 48 V to PoL conversion

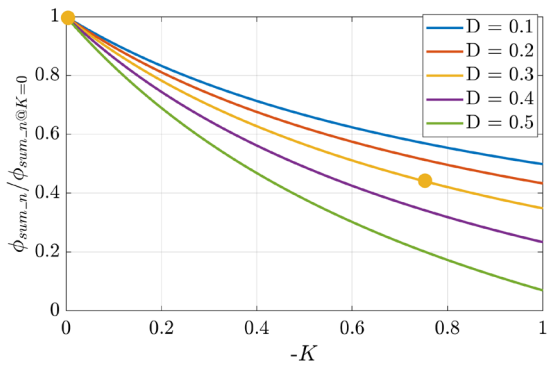


Zichao Ye, 2020 COMPEL

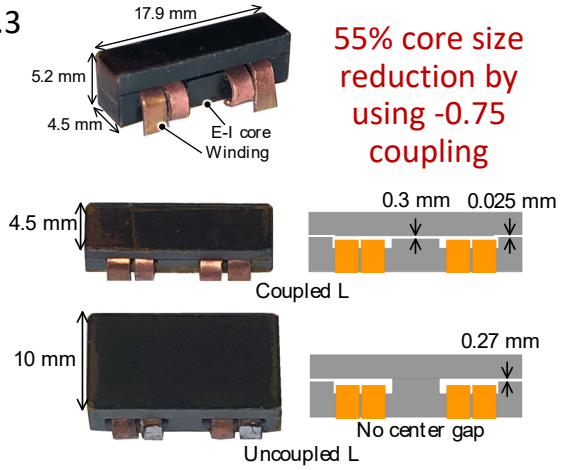
- In Point-of-Load (PoL) applications, inductors usually occupy >50% total volume
- **A general core-size model** is desired to evaluate the duty-ratio advantage of hybrid converters and guide magnetic design

Hardware Implementation

Modeled $\Phi_{sum_n}/\Phi_{sum_n@K=0}$ versus −K at α = 0.3



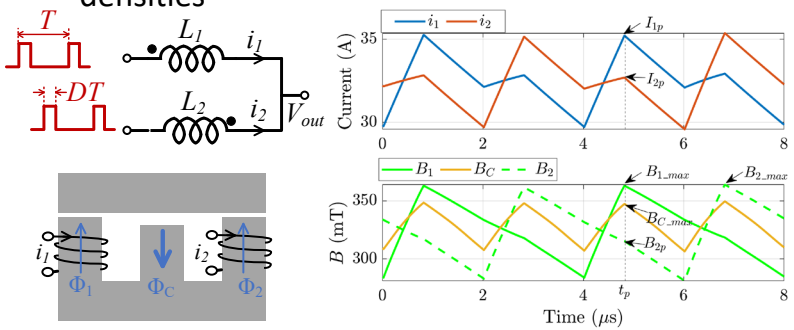
K: coupling coefficient



55% core size reduction by using -0.75 coupling

Proposed Method and Result

- 2-phase coupled inductors: schematic, core structure, current waveforms, and flux densities



- Total flux is proportional to core size and calculated by:

$$\begin{bmatrix}\Phi_{1_max}\\ \Phi_{2p}\end{bmatrix}=\begin{bmatrix}L_s & KL_s\\ KL_s & L_s\end{bmatrix}\begin{bmatrix}I_{1p}\\ I_{2p}\end{bmatrix}/N$$

$$\Phi_{sum_N}=\frac{\Phi_{sum}f_{sw}N}{V_{out}}=\frac{4}{\alpha(1-K)}-\left(\frac{4}{\alpha}+2\right)D+\frac{3}{2}$$

α: ripple factor, defined by the peak-to-peak inductor current over the maximum dc current

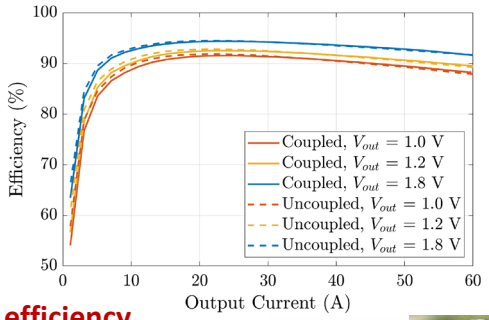
Experimental Results

Converter specifications	
V_{in}	48 V
Max. V_{out}	1.8 V
Max. D	0.3
Max. I_{out}	65 A
f_{sw}	250 kHz
α	0.3
Design 1: coupled inductors	
K	-0.75
L_s	800 nH
Design 2: uncoupled inductors	
L	517 nH

Converter performance summary

	Efficiency at 48 V input and 1.8 V output	Power density & Dimensions
Coupled L (This work)	**Peak: 94.4% Full load: 91.5%**	**474 W/in³ 26×18.4×7.8 mm**
Uncoupled L (This work)	Peak: 94.5% Full load: 91.6%	391 W/in³ 31.5×18.4×7.8 mm
[1] using commercial discrete L	Peak: 94.0% Full load: 91.3%	329 W/in³ 29×18.4×10.1 mm

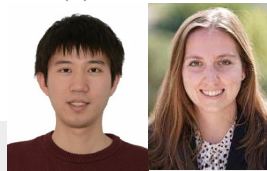
Measured efficiency including gate drive loss



The converter with coupled L achieves **0.4% higher peak efficiency** and **44% higher power density** compared to the discrete counterpart.

Reference: T. Ge, R. Abramson, Z. Ye, and R. C. N. Pilawa-Podgurski, "Core Size Scaling Law of Two-Phase Coupled Inductors – Demonstration in a 48-to-1.8 V Hybrid Switched-Capacitor MLB-PoL Converter," 2022 APEC.

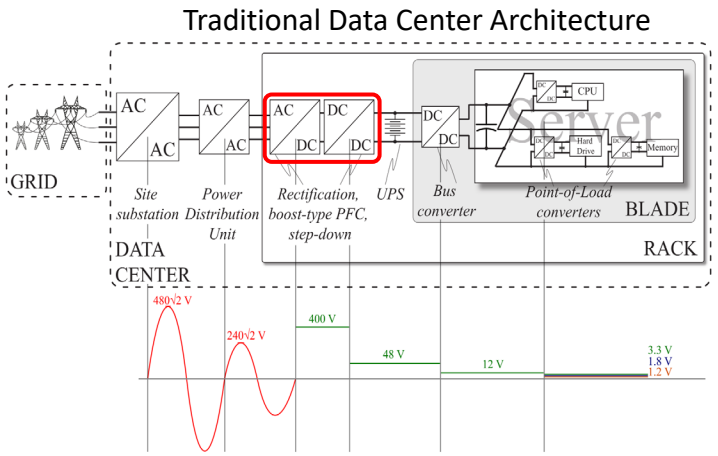
Ting Ge, Rose Abramson Email: {gting, rose_abramson}@berkeley.edu



High Efficiency 240 Vac to Load Data Center Power Delivery Topologies and Control

Berkeley Power and Energy Center

Motivation and Application

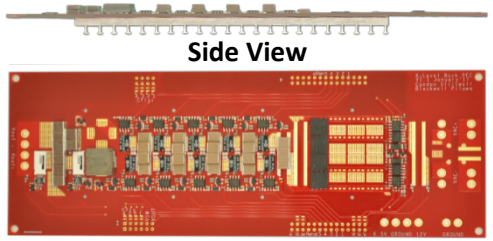


Traditional data center power factor correction (PFC) units boost voltage before rectification and step-down

Proposed: A one-stage single-phase ac-dc converter (240 Vac to 48 Vdc) with PFC

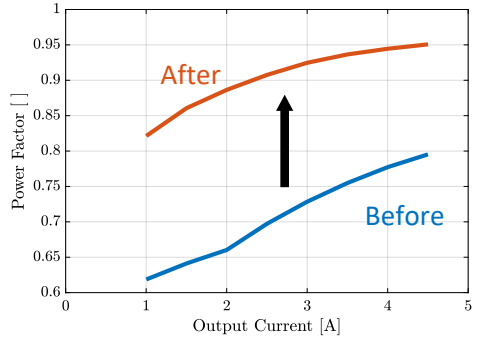
Metrics	Existing	Proposed
Peak Efficiency	94 %	97.8 %
Power Density	0.33 kW/L	7.5 kW/L

Hardware Prototype



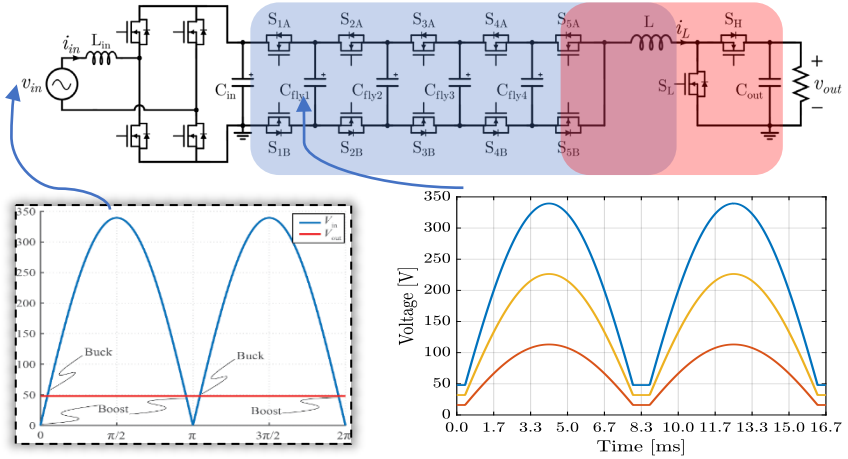
Operating Parameters	
Number of Levels	6
Switching Frequency	40 kHz
Output Current	4.5 A

Current Compensation to Improve Power Factor



Displacement current from C_{in} and C_{fly} leads to a phase shift in the input current, degrading the power factor. Our improved control algorithm compensates for this current to improve power factor [1].

Challenges and Solutions



Converter will buck or boost depending on point in AC input line cycle

Flying capacitor voltages vary with ac line cycle → unique challenges with capacitor balancing

Buck: S_H ON, S_L OFF; $S_{\{1,2,3,4,5\}A}$ and $S_{\{1,2,3,4,5\}B}$ modulate

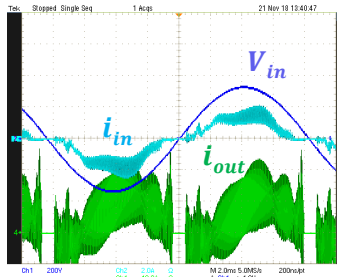
Boost: $S_{\{1,2,3,4,5\}A}$ ON, $S_{\{1,2,3,4,5\}B}$ OFF; S_L and S_H modulate

Preliminary prototype tests buck functionality, so that the converter is off when $|V_{in}| < V_{out}$.

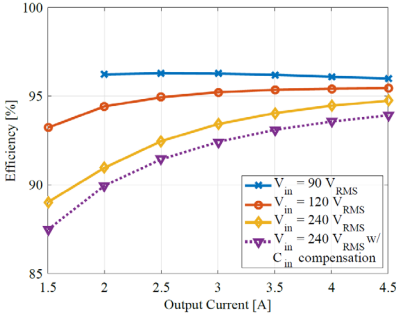
The converter relies on a stiff 48 V at the output (i.e. the UPS)

Experimental Verification

Operating Waveforms



Efficiency Curves



Performance Specifications	
Efficiency	94.8% at 240 Vac, 250 W
Volume (Box)	2.45 in³
Power Density	163 W/in³ (w/o heatsink) 79 W/in³ (w/ heatsink)

References:
[1] E. Candan, A. Stillwell, N. Brooks, R. Abramson, J. Strydom, R. C. N. Pilawa-Podgurski, "A 6-level Flying Capacitor Multi-level Converter for Single Phase Buck-type Power Factor Correction," in *Proceedings of 2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2019.

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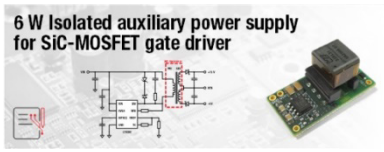
Advanced Techniques for Driving Floating Switches in the Flying Capacitor Multi-level converter

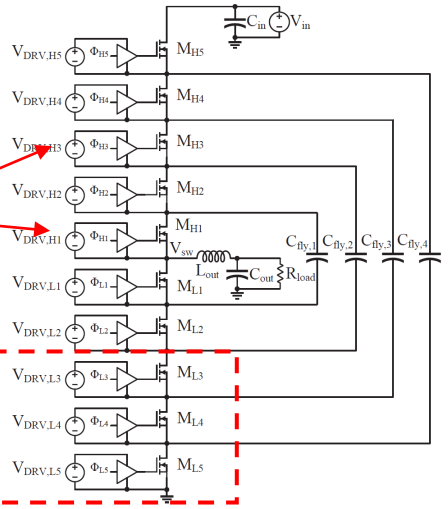
Berkeley Power and Energy Center

Motivation and Application

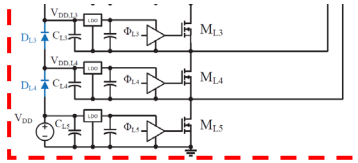
Floating switches need floating power supplies

- Typically use isolated power supply for each switch
- Large volume (due to isolation transformer) and high cost





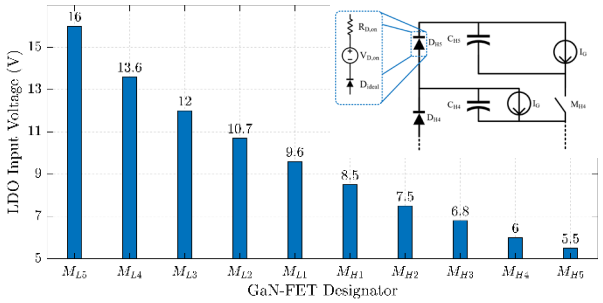
"Cascaded bootstrap" proposed for reduced volume and cost



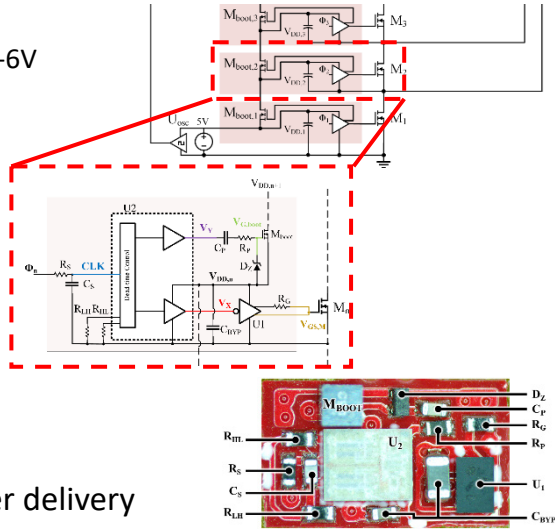
Challenges with Bootstrap Solution and Innovations

Voltage drops in bootstrap diodes require supply significantly higher than gate-drive voltage

- Local regulation necessary for driving GaN-FETs at 5-6V



Synchronous Bootstrapping

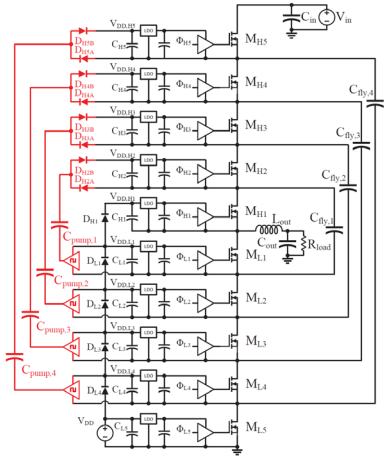


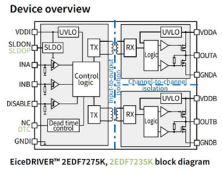
Replace bootstrap diodes with FETs

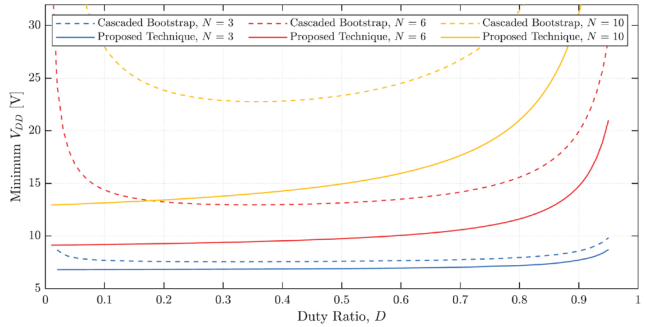
- Reduced voltage drop, bidirectional power delivery

Charge-Pump Technique

Oscillator driven charge pump: can be easily integrated with existing isolated drivers





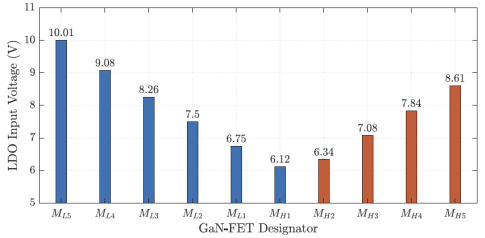


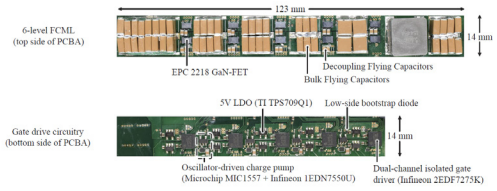
Can operate at low duty ratios with reduced gate-drive supply

- Higher gate drive efficiency

Experimental Verification

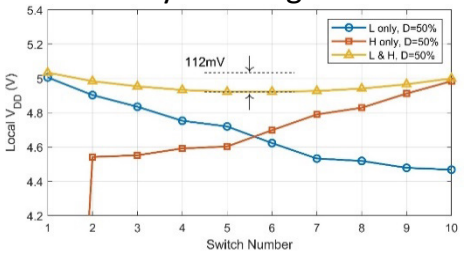
Reduced gate-drive supply with high-side switches fed by charge-pump





Synchronous bootstrapping:

- power delivery from high and low-sides



References:
[1]Z. Ye, et al., "Improved Bootstrap Methods for Powering Floating Gate Drivers of Flying Capacitor Multilevel Converters and Hybrid Switched-Capacitor Converters," in IEEE Transactions on Power Electronics.
[2] R. K. Iyer, N. M. Ellis, Z. Ye and R. C. N. Pilawa-Podgurski, "A High-Efficiency Charge-Pump Gate Drive Power Delivery Technique for Flying Capacitor Multi-Level Converters with Wide Operating Range," 2021 IEEE Energy Conversion Congress and Exposition (ECCE).
[3] N. M. Ellis, R. Iyer and R. C. N. Pilawa-Podgurski, "A Synchronous Boot-strapping Technique with Increased On-time and Improved Efficiency for High-side Gate-drive Power Delivery," 2021 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)

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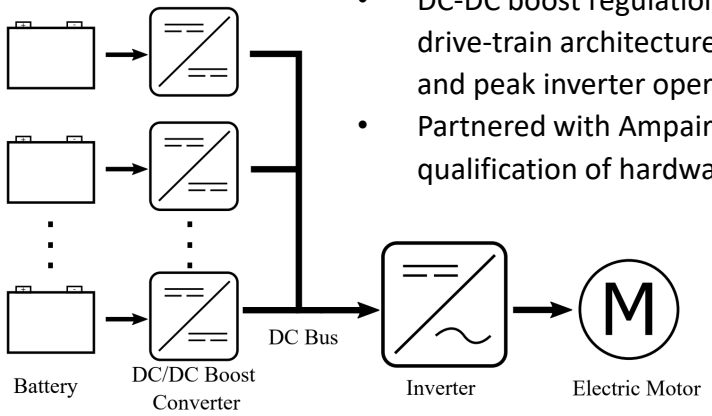
Design and Implementation of a (Flying) Flying Capacitor Multilevel Converter

Berkeley Power and Energy Center

Motivation and Application

- DC-DC boost regulation stage added to hybrid electric drive-train architecture to allow variable battery voltage and peak inverter operation.
- Partnered with Ampaire and ARPA-E for flight qualification of hardware.

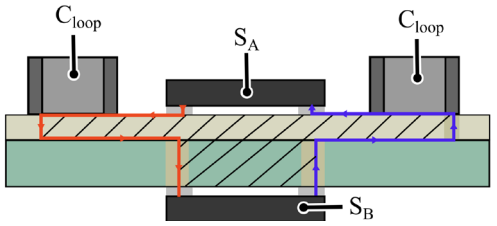


Proposed drivetrain architecture.

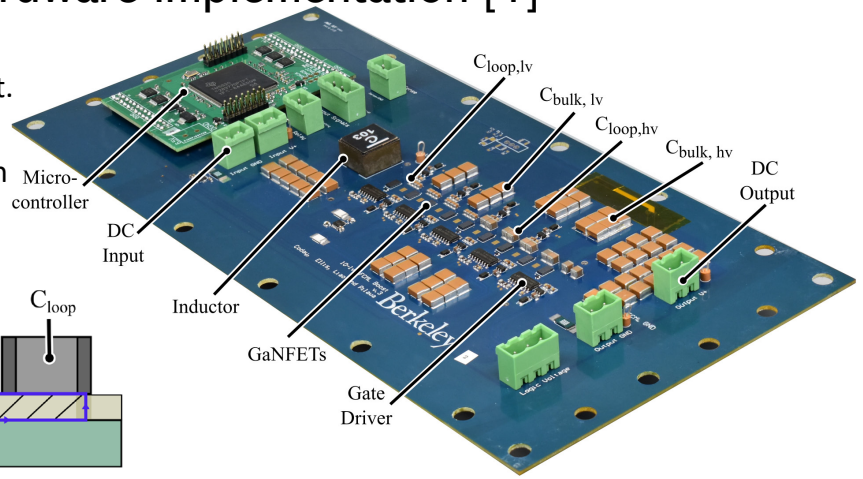
Ampaire EEL flight.

Hardware Implementation [1]

- 10-level FCML design is light-weight and compact.
- Modified electrically thin commutation loop design decreases parasitic inductance.

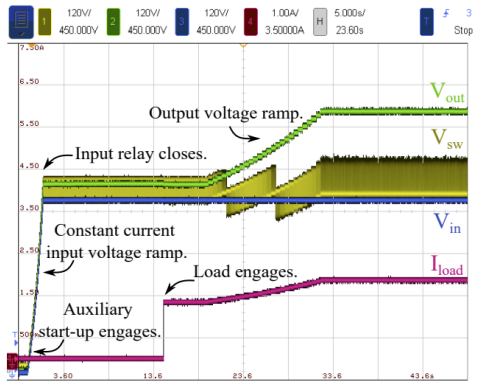


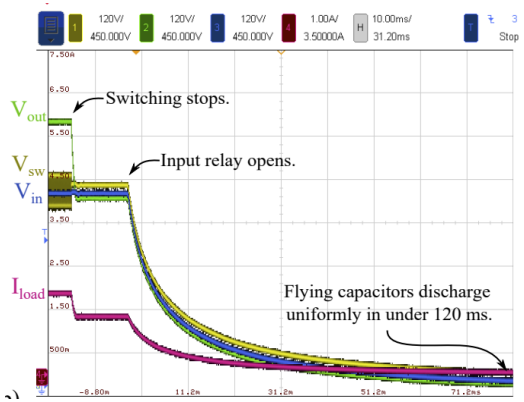
Commutation loop rendering.



10-level FCML labelled hardware prototype.

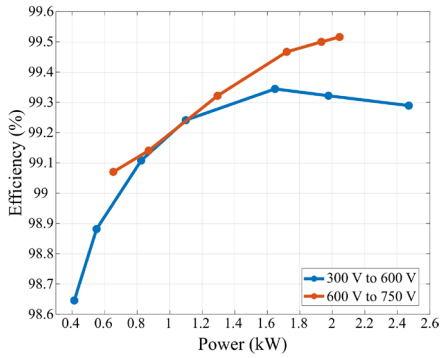
Challenges and Solutions [2]



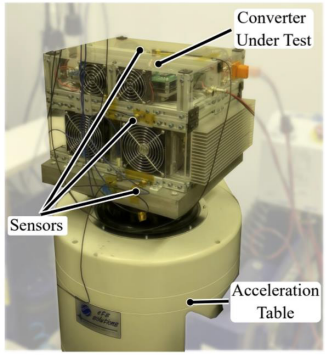


- Start-up auxiliary circuit and control allows for safe start-up at high voltages.
- Careful shutdown control of FCML is demonstrated as to not over stress switches.

Experimental Results [3]

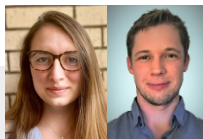


Measured efficiency (including gate drive losses).



Vibration test set-up.

Aircraft Installation

[1] S. Coday, N. Ellis, Z. Liao, and R. C. N. Pilawa-Podgurski, "A Lightweight Multilevel Power Converter for Electric Aircraft Drivetrain.," in 2021 IEEE Energy Conversion Congress and Exposition (ECCE), 2021.
[2] S. Coday, N. Ellis, Z. Liao, and R. C. N. Pilawa-Podgurski, "Modeling and Analysis of Shutdown Dynamics in Flying Capacitor Multilevel Converters.," 2021 IEEE Workshop on Control and Modeling for Power Electronics (COMPEL), 2021.
[3] S. Coday, N. Ellis, N. Stokowski, and R. C. N. Pilawa-Podgurski, "Design and Implementation of a (Flying) Flying Capacitor Multilevel Converter," in 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), 2022.

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