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Prof. Jessica Boles, Co-Director, Power Electronics

Prof. Duncan Callaway, Principal Investigator, Power Systems

Prof. Emeritus Seth Sanders, Principal Investigator, Power Electronics

Dr. Sascha von Meier, Principal Investigator, Power Systems

Prof. Costas Spanos, Principal Investigator, Energy Efficiency
Research Programs

- Power Components and Devices
- Circuit Topologies and Control
- Grid Integration – Systems and Technologies
Application Areas

Electric Transportation and Charging Infrastructure
Application Areas

Datacenter, Consumer Electronics, and Power Management
Integrated Circuits
Renewables, Storage, and Grid-Connected Systems
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- Additional CM projects: $100,000 annually
- For more information and how to join, please visit bpec.berkeley.edu
Motivation and Application
- Commercial aviation benefits from electric & hybrid vehicles
- Electric engines can be quieter and cleaner than jet engines
- Electric drive system must be power-dense and efficient
- Advanced power dense motors need low THD, high frequency drive current

NASA MEA Roadmap
- NOx emissions 80% reduction
- Fuel consumption 60% reduction
- Acoustic noise 71dB reduction

High Power Dynamometer
- Dyno incorporates two low-inductance Emrax 348 machines (peak power: 260 kW)
- Testing validated the Flying Capacitor Multilevel Converter’s (FCML) strength in a realistic motor drive system

Experimental Verification or Other
- Prototype meets NASA performance metrics for turbo-electric aircraft
- Integration of advanced thermal management will boost maximum output power and efficiency
- Modular design provides for power scalability and fault resiliency
- Next steps: verification of floating-point motor control algorithm and high-power dyno and next generation inverter hardware development

<table>
<thead>
<tr>
<th></th>
<th>NASA Target</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak Efficiency</td>
<td>99%</td>
<td>98.95%</td>
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<tr>
<td>Power Density</td>
<td>19 kW/kg</td>
<td>38.4 kW/kg</td>
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</tbody>
</table>

References:
Motivation and Application

- Air travel accounts for ~200 million tons of CO₂ emissions annually (3% of US greenhouse gas emissions)[1]
- Air travel demand is expected to double every fifteen years
- Electrification of flight requires efficient, lightweight, and reliable power conversion
- Hardware must be flight qualified

Proposed Solution

- Regulating boost DC-DC converter facilitates varying battery voltage and inverter load demand

Hardware Prototype

- Snubbers enable decreased overlap loss without sacrificing conduction path
- Paralleled switches enable increased areal power density
- Derated energy density metric used to optimize flying capacitor part/count
- Custom inductor achieves 3x mass reduction

Modeled Performance

- #X = number or parallel switches

Loss Breakdown

P_{cond} (39%)  P_{total} (12%)  P_{core} (2%)  P_{winding} (12%)  P_{on/off} (5%)  P_{gate} (10%)  P_{ESR} (1%)  P_{CROSS} (32%)

Empowering Future Electric Aircraft with a Flying Capacitor Multilevel Inverter Utilizing Optimal Passive Components

Motivation and Application

- Air travel accounts for ~200 million tons of CO₂ emissions annually (3% of US greenhouse gas emissions)[1]
- Air travel demand doubles every fifteen years
- Electrification of flight requires efficient, lightweight, and reliable power conversion

FCML with Optimal Passive Component Selection

- 10 kW, 800 V, 14-level FCML
- Sandwich-style layout with two printed circuit boards
- Ultra-thin design, only 8 mm thick!

Capacitor Sizing

- Conventional approach utilizes large, identical capacitors
- Proposed approach optimally selects unique capacitors for each flying capacitance
- Enables > 50% reduction in size

Hardware Prototype

- Highest power density among state-of-the-art aircraft inverters
- Excellent capacitor balancing and low output distortion despite the small size of the converter

Experimental Verification

- 100% Efficiency

References:

Logan Horowitz  |  Email: logan_h_horowitz@berkeley.edu
Tethered Power Systems for Lunar Mobility and Power Transmission (TYMPO)

Motivation and Application
Extreme terrain capable robots will enable further exploration on sites such as pits on the moon and Martian landscape. Tethered power systems have been proposed to power these small rovers; however, they require high voltage DC power [1].

Challenges
High voltage switches are difficult to use in space due to radiation effects. Additionally, the high voltage conversion ratio makes it difficult to design a compact and efficient power converter. Therefore, multilevel topologies offer promising solutions [2].

System Architecture (Flying Capacitor Multilevel Converter)
- Comparison of cascaded structure consisting of resonant flying capacitor multilevel converter (FCML) and regulating FCML (resonant FCML + regulating FCML) vs single-stage FCML converter
- Bus capacitance requirement diminishes benefits of cascaded structure

Passive Mass Minimization
- Comparison of 8-level regulating mode FCML converter with a resonant mode FCML converter, demonstrating the advantages of a resonant converter in terms of passive component mass
- Each converter operating point is optimized for minimal mass based on the peak energy storage requirements of the passive components

Hardware Verification
840 V-to-120 V space-rated FCML converter to verify:
- PCB structure (Gate drive daughterboard)
- Part selection
- Thermal solutions
- Mass optimization

References:

Student: Elisa Krause, Maggie Blackwell, Logan Horowitz
Email: {elisa_Krause, blackwell, logan_h_horowitz}@berkeley.edu
**On the Size and Weight of Passive Components: Scaling Trends for High-Density Power Converter Designs**

**Motivation and Application**

To build a high-density power converter, practicing engineers need to use passive components with the highest density.

- A component survey finds **Volumetric Energy Density**.
  - Visualized to assist component selection.
- But how to estimate **Gravimetric Energy Density**?
  - No component mass on most datasheet.

**Capacitor Volumetric vs. Gravimetric Energy Density**

$$\rho_V = \frac{2\ V_C^2}{\ V_{Vol}}$$

**Gravimetric Energy Density**

$$D(V_C, C) = \frac{\text{Mass}}{\text{Vol}}$$

**Inductor Volumetric vs. Gravimetric Energy Density**

$$D = k \cdot V_I^x \cdot L^y$$

**Mass data** was obtained through manual measurements of over 6,000 components.

**Power Fit Estimation for Specific Density (D)**

$$D = k \cdot L^a \cdot I^b$$

Enabling Buck-Type AC/DC Grid-Tied Rectifiers Using Flying Capacitor Multi-Level Converters with Advanced Control

Motivation and Application

Data center power consumption 1%+ of global electricity demand and growing [1]

Single-stage rectification
- Increased efficiency
- Greater power density

240 V_{ac} \rightarrow 48 V_{dc} \rightarrow 1 V_{dc} \rightarrow CPU

FCML and Active Flying Capacitor Voltage Balancing

6-Level Buck-Type FCML PFC Rectifier
- Reduced magnetics volume
- High FOM switches

Control Schematic

Experimental Verification

- Target Power Factor 0.97
- Passive Balancing 0.88
- Active Balancing 0.97+

References:

Rod Bayliss III Email: rodbay@berkeley.edu

Hardware

TI C2000 DSP (F28379D)

Background and Motivation

**Existing** two-stage lateral power delivery (LPD) architecture
- Large power distribution network (PDN) and high PDN losses
- Occupies a large area on the top side of the baseboard

**Proposed** single-stage vertical power delivery (VPD) architecture
- Much lower PDN losses
- Saves the topside area for high-speed communication and memories

Advantages of Switching-Bus-Based Architecture
- Does not require a large decoupling capacitor to maintain a stiff DC bus voltage
- One redundant switch can be removed on each switching bus while two stages are merged
- Ensures complete soft-charging operation

Proposed Switching Bus Converter (SBC)

**Hybrid switched-capacitor topology**
- Two 2-to-1 switched-capacitor (SC) front-ends
- Four series-capacitor buck (SCB) modules
- Two switching buses

**Hardware prototype**
- Good modularity
- Custom four-phase coupled inductor
- Efficient and compact gate drive circuitry

Experimental Results and Performance Comparison

- 92.4% peak system efficiency and 607 W/in³ power density (including gate drive loss and volume)

References:

Yicheng Zhu, Ting Ge, Nathan M. Ellis, and Jiarui Zou  Email: {yczhu, gting, nathanmilesellis, jiarui.zou}@berkeley.edu
48-to-6 V Cascaded Series-Parallel Converter for Intermediate Bus Applications

**Motivation and Application**

Data center power delivery has recently moved to a 48 V bus, which must be stepped down at the server racks. Commonly, this bus is stepped down to a 12 V intermediate bus, which is then converted to the low voltage, high current rails needed at the point-of-load (PoL). However, lower (i.e. 4-8 V) intermediate bus voltages have shown promise in increasing overall system efficiency by allowing the 2nd stage PoL converter to operate at lower input voltages, and therefore higher efficiency.

**Theory of Operation**

The 8:1 cascaded series-parallel (CaSP) converter consists of a 2:1 input stage merged with a 4:1 series-parallel converter. The multi-operating-phase operation allows the converter to achieve a high conversion ratio with fewer components compared to conventional two-phase hybrid switched capacitor circuits. The converter is operated above resonance to reduce RMS currents and make it less sensitive to capacitor tolerance variations.

**Converter Performance**

The 8-to-1 cascaded series-parallel (CaSP) converter consists of a 2:1 input stage merged with a 4:1 series-parallel converter. The multi-operating-phase operation allows the converter to achieve a high conversion ratio with fewer components compared to conventional two-phase hybrid switched capacitor circuits. The converter is operated above resonance to reduce RMS currents and make it less sensitive to capacitor tolerance variations.

**Experimental Validation**

The hardware prototype was designed using 25 V and 40 V Si MOSFETs (Infineon OptiMOS) and Class II ceramic capacitors. The inductor is recessed into the PCB to obtain a more power dense design.

- **Operating Parameters**
  - Phase Equivalent Circuits
  - Operating Waveforms
  - Schematic of 8:1 CaSP Converter
  - Efficiency vs. Load
  - Comparison with Contemporary State of the Art

**References:**

**Motivation and Application**

- **Power Flow:**
  - 90-240 Vac to 400 Vdc is a critical conversion stage for applications such as data center power delivery, electric vehicle charging, etc.
- **Ac-dc power factor correction**
  - Use of flying capacitors as energy storage greatly decreases volume of passive components and reduce filtering needs
- **Twice-line frequency power ripple buffering**
  - Use of active circuitry decreases capacitance requirement for twice-line frequency buffering and further promoted volume reduction

**Hardware Implementation**

- **Flying capacitor multi-level”(FCML) converter as the power factor correction stage**
- **Series-stacked Buffer as energy buffer stage**
- **Modular stack-up of full system**

**Design Objectives**

- **High Power Density**
  - Reduce system volume via new circuit topologies and control
- **Reduced Weight**
  - Custom 3D-printed cold-plate (collaboration with Miljkovic Group at UIUC)
  - 3D printed cold-plate Printed Fluid Channels

**Experimental Verification**

- **Parameter**
  - Peak tested power: 6.1 kW
  - Peak efficiency (1.1 kW): 99.1%
  - Efficiency @ 6.1 kW: 97.8%
  - PFC up to 1.5 kW: > 99.6%
  - Box-volume power density with cold plate: 7.6 kW/L

**Box-volume power density with cold plate:**

- **400 Vdc to 240 Vac system waveforms at 6.1 kW**
- **THD up to 1.5 kW**

**References:**


An EMI-Compliant and Automotive-Rated 48 V-to-PoL Dickson-Based Hybrid Switched Capacitor DC-DC Converter

Motivation and Application
Data center power delivery and automotive powertrains tending towards a 48 V distribution rail
- Higher intermediate bus voltages minimize losses and reduce cabling weight
This work demonstrates the merit of hybrid SC topologies for use in 48 V automotive systems
- Regulating Dickson-based hybrid SC topology
- EMI mitigation techniques – filtering and spread-spectrum frequency modulation

Topology and Challenges
Hybrid switched-capacitor, 8-to-1 interleaved-input, single-inductor Dickson converter
- Differential input → continuous input current → reduced required input filter
- Inductor at output → filtering and EMI shielding at low side
- Inductor at output → voltage regulation
Challenges
- Split-phase switching necessary for soft-charging of the flying capacitors
- Automotive component selection
- High efficiency, power density, and CISPR 25 Class 5 EMI compliance

Hardware Implementation
Uses only automotive-qualified parts
Switch selection based on required function, both Si and GaN
EMI input filter and spread spectrum frequency modulation (SSFM) to reduce EMI

Experimental Results
Differential Mode (DM) EMI results

Bidirectional Power Transfer in Hybrid Switched-Capacitor Converter for 48V/12V Regulated Automotive Applications

Motivation and Application

Bidirectional DC-DC Converter

48V DC/DC 12V

Need:
- 48V battery should be able to deliver extra power to 12V battery based on increased load demand and vice-versa.

Challenges:
- Delivery of high current with high efficiency and high power density in both directions

Converter Topology

- 48V-to-12V regulated cascaded hybrid resonant-PWM converter [1]
- 1st stage uses a conventional doubler in resonant mode
- 2nd stage used two interleaved doublers operating in PWM mode.

Advantages of Proposed Control Technique

- Implements Natural Balancing of all flying capacitors.
- Achieves Soft-charging and soft-switching.
- Minimizes the size of the intermediate capacitor $C_{\text{mid}}$.

Hardware Demonstration and Results

Measured Efficiency at:
- Input voltage: 48 – 60V
- 80 A full-load current
- Regulated 12 V output

- 80A, 99% peak eff. 3115 W/in$^3$ power density
- 21% loss and 63% size reduction over SOTA

(1) T. Ge, et. al., "A Regulated Cascaded Hybrid Switched-Capacitor Converter with Soft-Charging and Zero Voltage Switching for 48-to-12-V," 2023 IEEE APEC.

Nagesh Patle, Ting Ge
Email: {nageshpatle, gting}@berkeley.edu
**Piezoelectrics as Passive Components**

Magnetics present fundamental size and performance challenges at small scales.

Piezoelectrics store energy in mechanical compliance and inertia.

- High power density
- High efficiency
- Planar form factor
- Batch fabrication
- Integration potential

Piezoelectrics are promising alternative passives for miniaturized power conversion.

**Converter Topologies Based on Piezoelectrics**

We develop converter topologies that leverage the advantages of piezoelectrics in a variety of applications.

- Piezoelectric-transformer-based dc-dc converter
- Hybrid piezo / switched capacitor converter

**Control for Efficient Utilization of Piezoelectrics**

We develop high-performance switching sequences and control strategies tailored to optimal utilization of piezoelectrics.

**Experimental Demonstration**

We experimentally demonstrate the high performance capabilities of piezoelectric-based power conversion.

PR-based dc-dc converter:

- Variied Gain, \( V_{in} = 100 \) V
- 80% V_{in}, 120% V_{out}, 6 W

Piezoelectric Passive Components for High-Performance Miniaturized Power Conversion

Piezoelectric Passive Components

- Magnetics present fundamental size and performance challenges at small scales
- Piezoelectrics store energy in mechanical compliance and inertia
- Piezoelectrics are promising alternative passives for miniaturized power conversion

Materials and Vibration Modes

- We evaluate the efficiency and power density capabilities of numerous piezoelectric materials and vibration modes

Structures and Design Optimization

- We develop design guidelines for achieving maximum efficiency and power density in a variety of piezoelectric component structures

Experimental Demonstration

- We experimentally demonstrate the drastic miniaturization capabilities of piezoelectrics compared to magnetics

Prof. Jessica Boles  
boles@berkeley.edu

---

**Fundamental scaling laws show that power density rises as volume decreases**

\[
\text{Power} \propto \alpha^2 \\
\text{Volume} \propto \alpha^3
\]

**Voltage**

\[
\text{Voltage} = \alpha
\]

**Efficiency**

\[
\text{Efficiency} = 1
\]

**Frequency**

\[
\text{Frequency} = \alpha^{-1}
\]

**Efficiency (%)**

\[
\log(\alpha)
\]

---

**Piezoelectric Power Density:** 1.01 kW/cm²

---

**Temperature:** <36 °C

---


Motivation and Application

Hybrid switched-capacitor converters
- More capacitive energy storage than inductive energy storage for size reduction
- Multiple low-voltage switches in place of a single high-voltage switch for efficiency improvement

Topology Comparison
- Analytical method to compare relative size and performance of various topologies
- Include the impacts of capacitor voltage ripple and inductor current ripple on passive component volume and switch stress

Passive Component Volume and Switch Stress Trade-Off

Increasing the switching frequency beyond resonance
- Trading $\uparrow$ switching loss for $\downarrow$ conduction loss
Increasing capacitance beyond minimal volume
- Trading $\uparrow$ volume for $\downarrow$ VA rating (efficiency)

Impacts of Switching Frequency and Conversion Ratio on Minimal Passive Volume [1]

- Series-Parallel has smaller passive volume $\rightarrow$ Higher power density
- Increasing $\Gamma = \frac{f_{SW}}{f_{RES}}$ $\rightarrow$ smaller passive volume $\rightarrow$ Higher power density

Validation of Analytical Model

Passive component volume for varied capacitance to validate minimal volume method

References:
Background and Motivation

- Insufficient terminal capacitances can greatly affect converter efficiency
- Bulky terminal capacitors become the bottleneck of converter miniaturization

Modeling Derivation and Effect Analysis

Simplified circuit model and general output impedance model

Output impedance of a 2-to-1 pure SC converter with different $C_{in}$ and $C_{out}$

Output impedance of a 2-to-1 resonant SC converter with different $C_{in}$ and $C_{out}$

Effect of terminal capacitances

Inductor current waveform of a 2-to-1 pure SC converter with different terminal capacitances

Inductor current waveform of a 2-to-1 ReSC converter with different terminal capacitances

Multi-Resonant Compensation Control (MRCC)

- Challenge: zero current switching (ZCS) is not achievable with 0.5 duty ratio with small $C_{in}$
- Solution: ensure ZCS operation with the optimal duty ratio and switching frequency
- Result: 5x terminal capacitance reduction without harming efficiency

Simulation and Experimental Verification

Key considerations

- Minimize switching loss
- Accurate parameter acquisition
- High accuracy

Multi-Resonant Compensation Control (MRCC)

References:


Yicheng Zhu, Zichao Ye  Email: {yczhu, yezichao}@berkeley.edu

Hardware prototype

Simulation

Experiment

(a) Hardware prototype

(b) Hardware prototype

Simulation

Experiment

Output impedance (Ω)

Switching frequency (MHz)

Inductor current waveform of a 2-to-1 ReSC converter with different terminal capacitances

Inductor current waveform of a 2-to-1 pure SC converter with different terminal capacitances

(a) Comparison of output impedance. (b) Inductor current waveform of the conventional control. (c) Inductor current waveform of MRCC.
Analysis of Phase Timings for a Zero-Voltage Switching, Split-Phase Hybrid Dickson Converter

Motivation and Application
- Dickson-based converters are popular for hybrid switched capacitor (SC) solutions due to the reduced switch stress as compared to other topologies [1].
- Applications: high-conversion ratio systems.
- 48 V bus architectures for data centers and automotive powertrains.
- Transistor switching losses can be significant share of overall losses, especially with trends towards faster switching frequencies.
- Soft-switching techniques, such as zero-current and zero-voltage switching (ZCS and ZVS) can be used to reduce these losses.

Challenges
- Phase-timings become non-trivial to determine.
- ZVS timings are also non-trivial.
- Non-linear switch output capacitance.
- Multiple switches with different blocking voltages.

Hardware
- 48 V-to-6 V prototype.
- Per-phase analysis of an equivalent LC network to determine phase-timings.
- Equivalent capacitance $C_{eq}$:
- Main phases: A network of the flying capacitors $C_1$-$C_7$.
- ZVS sub-phases: A network of linearized transistor output capacitances [2].

Experimental Verification
- Exemplary phase-timings and waveforms of a resonant Dickson converter achieving ZVS on all switches.
- Measured drain-source voltages showing ZVS for all switches.

References:

53 % loss reduction
6 % loss reduction

An efficiency comparison of ZVS to ZCS, as well as calculated timings to fixed timings.
Motivation and Application

Data Center Two-Stage Power Architecture

Resonant switched-capacitor (ReSC) converters have demonstrated competitive efficiencies and power densities for 48-V-to-12-V conversion in data centers [3].

Due to finite terminal filtering capacitances, the efficiency of ReSC converters is often maximized when they are precisely soft switched [4]. However, circuit nonidealities render ZCS and ZVS timing challenging to estimate creating the need for active control techniques.

Class II MLCC DC Bias Derating

Inductor Soft Saturation

Theory and Control

Non-Ideal ZCS

Non-Ideal ZVS

By sensing the switch node voltage, nonideal soft switching conditions can be detected. Complete ZCS or ZVS can then be achieved by implementing the proposed control scheme.

Control Flowchart

Experimental Verification

- Convergence to complete soft switching can be achieved from a wide range of initial switching frequencies.
- Active ZVS and ZCS control allow for higher peak efficiencies than the conventional open-loop techniques.

References:
Closed-Loop Split-Phase Control Demonstrated in Hardware

An added Split-Phase Control Loop detects “hard-charging” events and informs appropriate phase timing adjustments within a conventional FPGA-based clock generator.

Example: Phase Progression of the SDIH (Dickson-Type) Converter

The duration of all phases are fully constrained as a function of $V_{IN}$, $V_{OUT}$, $I_{IN}$, $f_{SW}$, & component values. The practical inclusion of loss and component derating/mismatch necessitates continuous and dynamic phase duration adjustments.

Motivation and Application

Hybrid Switched Capacitor (HSC) power converter topologies are being adopted in 48V to point-of-load (PoL) applications. Within the HSC converter class, Dickson-type converters [1] achieve the lowest Volt-Amp switch stress, indicative of a smaller semiconductor footprint for equivalent performance. However, some of these topologies require a non-conventional clocking scheme — recently coined as “split-phase switching” [2] — to ensure high efficiency is preserved. Executed in parallel with complimentary work in [3], this work presents a closed-loop split-phase control appropriate for regulating PoL converters [4]; overcoming a key obstacle to the deployment of a new and highly competitive class of hybridized power converter topologies.

Active Soft-Charging Control for Hybrid and Resonant Switched-Capacitor Converters

Motivation and Application

Dickson-derived converters are increasingly used for both fixed-ratio and direct-to-Pol applications in the datacenter and transportation space. They can achieve very low switch stress (i.e., Volt-Amp product), which means that lower-voltage (and therefore less lossy) switches can be used compared to other topologies for a given output power.

Split-Phase Control

Certain Dickson topologies require more complex split-phase control schemes [1] in order to achieve full soft-charging of all fly capacitors. Split-phase control timings can be complex to calculate and vary depending on component tolerance, circuit non-idealities, and operating condition, necessitating active control [2], [3].

Capacitor Losses: Hard-Charging vs. Soft-Charging

**Hard-charging:** large charge redistribution loss, spiky currents.

**Soft charging:** no charge redistribution loss, smooth / resonant currents.

**Phase 1 Split-Phase Operation**

If the (1a,1b) and (2a,2b) transitions occur at the wrong time, hard-charging occurs, resulting in current spikes and discontinuous capacitor voltages.

These voltage steps can be sensed, allowing the controller to auto-tune split-phase times to achieve soft-charging operation.

**Phase 1a**

- \( V_{c1} \)
- \( V_{c2} \)
- \( V_{c3} \)
- \( V_{c4} \)
- \( V_{c5} \)
- \( V_{c6} \)
- \( V_{c7} \)

**Phase 1b**

- \( V_{c1} \)
- \( V_{c2} \)
- \( V_{c3} \)
- \( V_{c4} \)
- \( V_{c5} \)
- \( V_{c6} \)
- \( V_{c7} \)

References:

Analog Sensing Circuitry

- Differential capacitor voltage sensed and signal-conditioned
- Slope detect circuit triggers on large step discontinuities
- Polarity of step discontinuity shows whether split-phase timing is too short or too long

Experimental Verification

- An 8-to-1 resonant Dickson converter was used for validation.
- The control scheme was able to converge on soft-charging split-phase timing when 1) initialized in a hard charging-condition, and 2) when enabled during load step transients.

**Steady-State Convergence**

- Smooth capacitor voltages signify soft-charging operation

**Experimental Setup**

- 48 V input
- 6 V output
- 10 A maximum output current

Contact:
Rose Abramson, Sahana Krishnan, Maggie Blackwell
Email: {rose_abramson, sahana_krishnan, blackwell}@berkeley.edu

Operating Conditions

- \( V_{in} \): 48 V
- \( V_{out} \): 6 V
- \( I_{out,max} \): 10 A
Closed-Loop Balancing Control and Capacitor Voltage Estimation for the Flying Capacitor Multilevel Converter

Balancing Control Motivation
Open-loop balancing of capacitor voltages is unreliable
• Capacitor voltages during large-signal transients exhibit
  underdamped dynamics
• Peak switch stress may be greater than \( \frac{V_{in}}{N-1} \) and can
  cause switch overvoltage in high-performance designs
  using low-voltage switches

Closed-Loop Control
• Model average behavior of FCML converter to obtain “plant” for control
• Structure of plant informs controller design: duty ratios can be controlled
differentially to steer capacitor voltages
• Balancing controller runs in parallel with controller(s) regulating load voltage
• Closed-loop system is decoupled – controllers operate without mutual interaction

Natural Balancing

Capacitor Voltage Estimation
• Active balancing requires measurement of capacitor voltages
• Measuring each capacitor voltage with its own differential sensor is expensive
• Can instead measure switched-node voltage with single-ended sensor and
calculate capacitor voltages
• Solve system of equations iteratively with reduced computation burden
• Demonstrated on industry-standard Texas Instruments C2000 DSP

Closed-Loop Balancing Control and Capacitor Voltage Estimation

• Active balancing ensures capacitor voltages track nominal values during
  supply transients
• Single-sensor estimation of capacitor voltages is reliable and low-cost

References:
A Hybrid Switched-Capacitor Solar Microinverter Utilizing a Fixed-ratio Resonant DC-DC Stage and Flying Capacitor Multi-level DC-AC Stage

Motivation and Application
Hybrid Switched-Capacitor Converters
- The Cascaded Series-Parallel converter (CaSP) has been used as a power-dense dc-dc step-down solution in the 48V application space but is being adapted use as a boost stage [1].
- The flying capacitor multilevel converter (FCML) can be used to step down the

System Architecture

Three sub-intervals of one switching cycle, each with a unique resonant LC tank impedance [2].
- Achieves ZCS, partial ZVS.
- Can be used as stand-alone startup circuitry.

Full microinverter concept.

Rooftop solar requires efficient and power dense solutions to convert power for use in homes and at the grid.

Example inverter: Enphase IQ8

CaSP System Specifications
- 35-40V input
- 350-400V, 500W output
- System able to produce 240 Vac output at light load
- CaSP achieves ZCS during full system operation at 240 Vac output

FCML System Specifications
- 350-400V input, 500W+
- Sensing for control included on this board.
- 2nd revision coming soon

Experimental Validation

Peak efficiency with 255 Vac output at light load: 93.5%

System waveforms with 240 V_ac output

References:
# A Charge Injection Loss Compensation Method for a Series-Stacked Buffer to Reduce Current and Voltage Ripple in Single-Phase Systems

## Motivation and Application

The Series-stacked buffer (SSB) is an active buffer topology that achieves high energy utilization and greatly decreases the power conversion system volume without comprising efficiency [2]. However, there can be a large amount of residual ac current ripple on the dc bus due to SSB’s control methodology that injects real power through the reactive buffer branch. This control is required to charge the C2 capacitor in the SSB that acts as a dc source for a full-bridge converter. Specifically, this ripple gets worse in applications with low source impedance, such as battery systems.

## Proposed “Charge Injection” Method

The Charge Injection method has a separate branch that handles real power delivery while the rest of the SSB handles the reactive power buffering. As a result, the dc-link current ripple is greatly reduced.

## Hardware

### Component Parameters

<table>
<thead>
<tr>
<th>Component</th>
<th>Part No.</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1 – S4</td>
<td>EPC2033</td>
<td>150 V, 6 mΩ</td>
</tr>
<tr>
<td>SCl</td>
<td>GaN Systems GS66506T</td>
<td>600 V, 2 A</td>
</tr>
<tr>
<td>DCI</td>
<td>ON Semiconductor MURS160T3G</td>
<td>650 V, 67 mΩ</td>
</tr>
<tr>
<td>LC1</td>
<td>Coilcraft MSS11210-104</td>
<td>100 μH</td>
</tr>
<tr>
<td>C1</td>
<td>TDK B32524Q1686K000</td>
<td>100 V, 68 μF x 3</td>
</tr>
<tr>
<td>C2</td>
<td>TDK B32776G4406K000</td>
<td>450 V, 40 μF x 2</td>
</tr>
</tbody>
</table>

The real power injection causes large ac current ripple along the dc-link. (24% ac current ripple shown at 1.5 kW at 400 Vdc).

## Experimental Verification

The peak-to-peak ac current ripple is reduced:
- By maximum of 5.3x
- And average of 4.3x
- 3x at peak load

Charge Injection method achieves an average efficiency of 99.4% across all loads.

## References


Student Name: Kelly Fernandez, kefernandez@berkeley.edu
Utilizing Harmonic Injection to Reduce Energy Storage in a Single-Phase Active Energy Buffer

**Motivation**

- Single-phase power converters rated for high power applications require reactive buffering on the dc bus to maintain a constant and clean dc power input or output. Often this is a bulky electrolytic capacitor.
- [1] found that buffer storage requirements for a passive buffer could be reduced 56% for the addition of allowable 3rd and 5th harmonics.
- We apply this harmonic injection method for energy storage reduction in the capacitors of the series-stacked buffer (SSB), which is a power-dense alternative to the conventional capacitor solution.

**Challenges and Control**

- Determining the expected voltage ripple on each of the capacitors is nontrivial.
- Figure out how to control an active buffer when additional harmonics are added to the system.

**Energy storage in buffer during a twice-line frequency cycle.**

\[
W_{\text{store}} = \int_0^{\frac{T}{2}} P_{\text{bus,}f}(t) \, dt
\]

\[
W_{\text{store}} = \frac{1}{2} C V_{\text{max}}^2 - \frac{1}{2} C V_{\text{min}}^2
\]

The SSB is an active buffer that combines a primary energy buffer capacitor with an H-bridge. This permits a larger voltage ripple across the main energy storage capacitor maximizing the amount of energy buffered, and subsequently the energy utilization ratio [2].

**Experimental Verification**

55% reduction in required energy storage split between two capacitors. In an example case, \( C_1 \) can be reduced from \( 60 \mu\text{F} \) to \( 34 \mu\text{F} \), and \( C_2 \) from \( 27 \mu\text{F} \) to \( 20 \mu\text{F} \) for same dc-bus voltage ripple [3].

References:

Francesca Giardine, Nathan Brooks, Kelly Fernandez

Email: fgiardine@berkeley.edu
Advanced Switching Cell Design Techniques

Motivation and Application

Power converters operate by switching between different circuit states. Ideally, the switching transitions would be instantaneous and lossless. In reality, parasitic effects cause switching losses, voltage overshoot, and electromagnetic interference. Advanced design techniques are presented here, which mitigate these effects and enable unprecedented performance.

Interleaved Commutation Loop Layout [2]

Commutation loop inductance is critical to switching performance. Advanced layout techniques can be utilized to reduce this inductance.

Interleaved hybrid decoupling capacitor loops with electrically thin vertical bulk capacitor loop

Optimal Decoupling Capacitor Sizing [1]

Determined optimal decoupling capacitor size given load current and output capacitance of the device:

\[ C_D = 10 \times \max\left\{ C_{OS}, 2L_B f_{ML}/U_{ML}^2 \right\} \]

Decoupling Device [3]

For many applications, transistors with large through-hole packages are used, due to their high power handling capability. In this work, a small surface-mount gallium-nitride transistor is added to improve switching performance.

References:


Logan Horowitz | Email: logan_h_horowitz@berkeley.edu
Motivation and Applications

- The intermediate bus converter in 48 V data center application requires high efficiency and high power density
- Regulation and isolation are not required

48 V data center power delivery architecture

- The intermediate bus converter in 48 V data center application requires high efficiency and high power density
- Regulation and isolation are not required

Proposed Topology

- Cascaded Multi-Resonant converter
- 1st stage uses only two switches to save space of active components, and gate drive level shifters

State-plane method is used to calculate multi-resonant inductor current

Experimental Results

- Dimensions: 17.3 × 23 × 6.6 mm, power density: 6000 W/in³ at 12 V output
- 80 A continuous output and 130 A - 2 ms transient output

Hardware Demonstration

- Dimensions: 17.3 × 23 × 6.6 mm, power density: 6000 W/in³ at 12 V output
- 80 A continuous output and 130 A - 2 ms transient output

Comparison with State-of-the-Art

- Measured efficiencies including gate drive loss

High Performance Single-phase Ac-dc Conversion with Advanced Topology and Control

Motivation and Application

- 90-240 Vac to 400 Vdc is a critical conversion stage for applications such as data center power delivery, electric vehicle charging, etc.
- Ac-dc power factor correction
  - Reduce boost inductor size
- Twice-line frequency power ripple buffering
  - Reduce buffer capacitor size

Challenges and Solutions

- The boost inductor size is reduced flying capacitor multilevel (FCML) topology
- An active buffer topology - series-stacked buffer (SSB) is implemented to reduce the buffer capacitor for twice-line frequency power ripple buffering

Hardware Implementation

- 90-240 Vac to 400 Vdc, 1.5 kW PFC converter [1]

Experimental Verification

- Total box-volume power density: 230 W/in³
- Peak efficiency: 98.9%
- 1.5 kW efficiency: 98.1%
- THD: < 5%
- Power factor: > 0.994

References:
**Theoretical Analysis**

- Systematically analyze and calculate switch and passive utilization
- Compare and select the most suitable topology depending on application and power level
- Develop control technique to achieve soft-charging and soft-switching

**Switch VA rating**

\[
\left( \sum_{\text{switches}} V_{\text{ds}} I_{\text{ds}} \right)
\]

**Total passives volume**

\[
\left( \frac{1}{2} \sum_{i} L_{i} \right)^{2} + \frac{1}{2} \sum_{i} C_{i} \]

**Practical Challenges and Solutions**

- Improved bootstrap and charge pump techniques to replace isolated dc/dc power supplies
- Achieving higher efficiency, lower cost and smaller footprint
- Working on system level circuit integration to further reduce size and cost

**Capacitor voltage balancing**

- Experimentally verified that source impedance and input capacitance can affect balancing drastically
- Even-level FCML converter has better natural balancing
- Gate drive voltage and signal mismatch can cause imbalance

**Cascaded Resonant Converter**

- Two-phase interleaved design
- Zero voltage switching technique
- Overcome the intermediate decoupling challenge of doubler topology
- Operate the tank in the inductive region to achieve ZVS, while improving tolerance of component variations

**Experimental Verification**

- Experimentally verified that source impedance and input capacitance can affect balancing drastically
- Even-level FCML converter has better natural balancing
- Gate drive voltage and signal mismatch can cause imbalance

**References:**


[3] Z. Ye, Y. Lei and R. C. N. Pilawa-Podgurski, ”A resonant switched capacitor based 4-to-1 bus converter achieving 2180 W/in3 power density and 98.9% peak efficiency,” APEC 2018

Student: Zichao Ye. Email: yezichao@berkeley.edu
An 83mA 96.8% Peak Efficiency On-Chip 3-Level Boost Converter with Full-Range Auto-Capacitor-Calibrating Pulse Frequency Modulation (ACC-PFM)

**Motivation and Applications**

High voltages are demanded to:
- Generate efficacious stimulations for bio-implantable devices
- Interface between low-voltage energy harvesters and batteries for wireless sensor network (WSN)
- Program memories for high operational speeds
- Drive LED strings efficiently

**Challenges and Solutions**

**Topology:** 3-level Boost Converter

- At least 3X reduction in conversion ratio, \( V_{O}/V_{IN} \)
- Hybrid SC converters merge the advantages of the conventional switched capacitor (SC) and switched inductor converters (e.g., Boost converter)
  - Achieve high power density
  - Mitigate charge sharing loss in SC converter
  - Retain the ability to employ low voltage

**Control:** ACC-PFM

- ACC-PFM is an integrated controller solution for both \( V_{OUT} \) regulation and capacitor balancing

- TSMC 65nm CMOS process
- 2.5V devices for 5.0V operation

**Measurement Results**

- Peak Efficiency: 96.8%
- Input Voltage: 0.3 – 3V
- Output Voltage: 2.4 – 5V
- Peak Output Current: 83 mA
- Peak Switch Current Density: 300 mA/mm²
- Switching Freq.: 0.5M – 45MHz

**Chip Implementation**

- TSMC 65nm CMOS process
- 2.5V devices for 5.0V operation

**References:**

Wen-Chuen Liu, Pei Han Ng, Robert C.N. Pilawa-Podgurski, “An 83mA 96.8% Peak Efficiency 3-Level Boost Converter with Full-Range Auto-Capacitor-Calibrating Pulse Frequency Modulation”, IEEE Custom Integrated Circuits Conf. (CICC), 2019.

Student: Wen-Chuen Liu  Email: joseph.wcliu@berkeley.edu
Motivation and Application

Increased power density of advanced CMOS nodes in embedded applications requires the power converters to have:

- Higher efficiency to extend the battery life
- Low loss to ease the thermal management
- Higher power density to match the technology
- Maintain performance at large conversion ratios

Typical Battery voltage 3.2 V to 4.2 V
Typical Load voltage 300mV to 1 V
Typical Load current several mA to several A

Challenges and Solutions

Utilized hybrid switched-capacitor (SC) converters.

Switched-Capacitor stage:
- Higher efficiency at large conversion ratios
- Lower rated devices for advance CMOS integration
- Poor regulation

Magnetic Buck stage:
- Achieve tighter regulation
- Lower voltage swing for smaller magnetics

Need higher utilization of passive and active devices:
- Dickson SC has good switch utilization and poor capacitor utilization
- Soft-charging through split-phase control increases capacitor utilization, enhances efficiency and lower switching frequency
- Smaller passives for faster transient response and tighter control

Hardware

- Implemented in CMOS 65nm bulk process
- Flip-Chip packaging for low parasitic
- Voltage borrowing gate drive to eliminate bootstrap capacitors and increase power density
- Active capacitor balancing and output regulation
- External flying capacitors and inductor
- High density interposer for uModule assembly

Experimental Verification

Maintained efficiency and power density:
- Across large conversion ratios
- Across large load current range

Characterization of Multi-layer Ceramic Capacitors under More Realistic Operating Conditions

Motivation and Applications

- Multi-layer ceramic capacitors (MLCCs) are a key enabling technology for high density power converters.
- Real losses in MLCCs can be reduced to equivalent series resistance (ESR).
- Data sheets do not provide loss information for realistic operating conditions.

Hardware Implementation

- ESR is dependent on frequency, DC bias, AC amplitude, temperature and harmonic content.
- A circuit was designed to be able to adjust frequency, current amplitude and DC bias of a high harmonic content waveform in order to test the effect on ESR.

Challenges and Solutions

\[ P_{\text{diss}} = \frac{1}{T_{\text{final}}} \left( k_{\text{oil}} \Delta \text{temp} + \int_0^{T_{\text{final}}} \frac{\text{temp}_{\text{oil}} - \text{temp}_{\text{amb}}}{R} \, dt \right) \]  

- Measuring loss with electrical characterization is inaccurate under desired operating conditions.
- A calorimetric method was implemented in order to accurately observe change in ESR.

Experimental Results

- With increased DC bias, the ESR linearly increases, this has been shown with several dielectric types as well as manufacturers.

References:


Student: Samantha Coday
Email: scoday@berkeley.edu
Hybrid Switched-Capacitor DC-DC Converters with Isolation

**Motivation and Applications**
- Hybrid switched-capacitor converters offer high power density but have been restricted to non-isolated applications
- Traditional isolation methods require bulky and heavy transformers
- Capacitive isolation presents a power-dense alternative to magnetic isolation
- Flying capacitors with high voltage rating act as isolation capacitors

**Challenges and Solutions**
- ZVS theoretically possible, but not successful at higher input voltages
  - Ongoing issue; we’ll spend more time investigating timing
- Light-load oscillations that damage converter at higher voltages
  - Current solution: avoid light load

**Theory of Operation**
- Capacitively isolated hybrid switched-capacitor converter based on [1], [2]
- Complete soft-charging of capacitors eliminates loss from transient inrush currents
- 50% duty cycle and two-phase operation
- Switch voltage stress independent of load

**Experimental Results**
- 94.1% peak efficiency, 2,010 W/in³ power density

---


Core Size Scaling Law of Two-Phase Coupled Inductors – Demonstration in a 48-to-1.8 V MLB (Multi-Level-Binary)-PoL Converter

Motivation and Applications

Multi-Level Binary (MLB) hybrid switched-capacitor converter for 48 V to PoL conversion

• In Point-of-Load (PoL) applications, inductors usually occupy >50% total volume
• A general core-size model is desired to evaluate the duty-ratio advantage of hybrid converters and guide magnetic design

Hardware Implementation

Proposed Method and Result

• 2-phase coupled inductors: schematic, core structure, current waveforms, and flux densities
• Total flux is proportional to core size and calculated by:

\[
\Phi_{\text{sum, } N} = \frac{\Phi_{\text{sum, } L_{\text{sw}}}}{N} \cdot \Phi_{\text{out}} = \frac{L_{s}}{\alpha(1 - K) \alpha + 2} \cdot \frac{D}{2} \cdot \frac{3}{2} 
\]

\[
\Phi_{\text{1-max}} = \frac{\Phi_{\text{2p}}}{L_{s}} = \frac{K_{L_{2}} L_{s} L_{s}}{K_{L_{2}}, L_{s}} \cdot \frac{I_{1}}{I_{2}} / N
\]

Zichao Ye, 2020 COMPEL

Experimental Results

Converter specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Design 1: coupled inductors</th>
<th>Design 2: uncoupled inductors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max. V_in</td>
<td>48 V</td>
<td>48 V</td>
</tr>
<tr>
<td>Max. V_out</td>
<td>1.8 V</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Max. D</td>
<td>0.3</td>
<td>0.3</td>
</tr>
<tr>
<td>Max. I_out</td>
<td>65 A</td>
<td>65 A</td>
</tr>
<tr>
<td>f_{sw}</td>
<td>250 kHz</td>
<td>250 kHz</td>
</tr>
<tr>
<td>K</td>
<td>0.75</td>
<td>0.75</td>
</tr>
<tr>
<td>L_s</td>
<td>800 nH</td>
<td>517 nH</td>
</tr>
</tbody>
</table>

The converter with coupled L achieves 0.4% higher peak efficiency and 44% higher power density compared to the discrete counterpart.


Ting Ge, Rose Abramson Email: {ting, rose_abramson}@berkeley.edu
High Efficiency 240 Vac to Load Data Center Power Delivery
Topologies and Control

Motivation and Application

Traditional data center power factor correction (PFC) units boost voltage before rectification and step-down.

**Proposed:** A one-stage single-phase ac-dc converter (240 Vac to 48 Vdc) with PFC.

### Challenges and Solutions

Converter will buck or boost depending on point in AC input line cycle.

Flying capacitor voltages vary with ac line cycle → unique challenges with capacitor balancing.

### Hardware Prototype

<table>
<thead>
<tr>
<th>Metrics</th>
<th>Existing</th>
<th>Proposed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak Efficiency</td>
<td>94 %</td>
<td>97.8 %</td>
</tr>
<tr>
<td>Power Density</td>
<td>0.33 kW/L</td>
<td>7.5 kW/L</td>
</tr>
</tbody>
</table>

- **Operating Parameters**
  - Number of Levels: 6
  - Switching Frequency: 40 kHz
  - Output Current: 4.5 A

- **Performance Specifications**
  - Efficiency: 94.8% at 240 Vac, 250 W
  - Volume (Box): 2.45 in³
  - Power Density: 163 W/in³ (w/o heatsink) 79 W/in³ (w/ heatsink)

- **References:**

- Current Compensation to Improve Power Factor

- Displacement current from $C_w$ and $C_f$ leads to a phase shift in the input current, degrading the power factor. Our improved control algorithm compensates for this current to improve power factor [1].

- **Experimental Verification**

- Preliminary prototype tests buck functionality, so that the converter is off when $|V_{in}| < V_{out}$.

- The converter relies on a stiff 48 V at the output (i.e. the UPS).
Advanced Techniques for Driving Floating Switches in the Flying Capacitor Multi-level converter

Motivation and Application
Floating switches need floating power supplies
• Typically use isolated power supply for each switch
• Large volume (due to isolation transformer) and high cost

“Cascaded bootstrap” proposed for reduced volume and cost

Challenges with Bootstrap Solution and Innovations
Voltage drops in bootstrap diodes require supply significantly higher than gate-drive voltage
• Local regulation necessary for driving GaN-FETs at 5-6V

Replace bootstrap diodes with FETs
• Reduced voltage drop, bidirectional power delivery

Charge-Pump Technique
Oscillator driven charge pump: can be easily integrated with existing isolated drivers

Can operate at low duty ratios with reduced gate-drive supply
• Higher gate drive efficiency

Experimental Verification
Reduced gate-drive supply with high-side switches fed by charge-pump

Synchronous bootstrapping:
• power delivery from high and low-sides

References:
Motivation and Application

• DC-DC boost regulation stage added to hybrid electric drive-train architecture to allow variable battery voltage and peak inverter operation.
• Partnered with Ampaire and ARPA-E for flight qualification of hardware.

Challenges and Solutions [2]

• Start-up auxiliary circuit and control allows for safe start-up at high voltages.
• Careful shutdown control of FCML is demonstrated as to not over stress switches.

Hardware Implementation [1]

• 10-level FCML design is light-weight and compact.
• Modified electrically thin commutation loop design decreases parasitic inductance.

Experimental Results [3]

Measured efficiency (including gate drive losses).

Samantha Coday, Nathan Ellis
Email: {scoday, nathanmilesellis}@berkeley.edu